

ZZZ1



SE000008600

# Compal Confidential

## Everest Schematics Document

Intel Merom Processor with Crestline + DDRII + ICH8M

2007-03-05

REV: 0.2

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**Model Name : Everest**  
**File Name : LA-3691P**



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE	SIGNAL							
	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

ID1	ID0	TEST
0(R744)	0(R745)	A-TEST
0(R744)	1(R742)	B-TEST
1(R741)	0(R745)	C-TEST

PANEL ID Table

R	Size
Ra (R743)	15W
Rb (R740)	14W

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

EC SM Bus1 address




Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

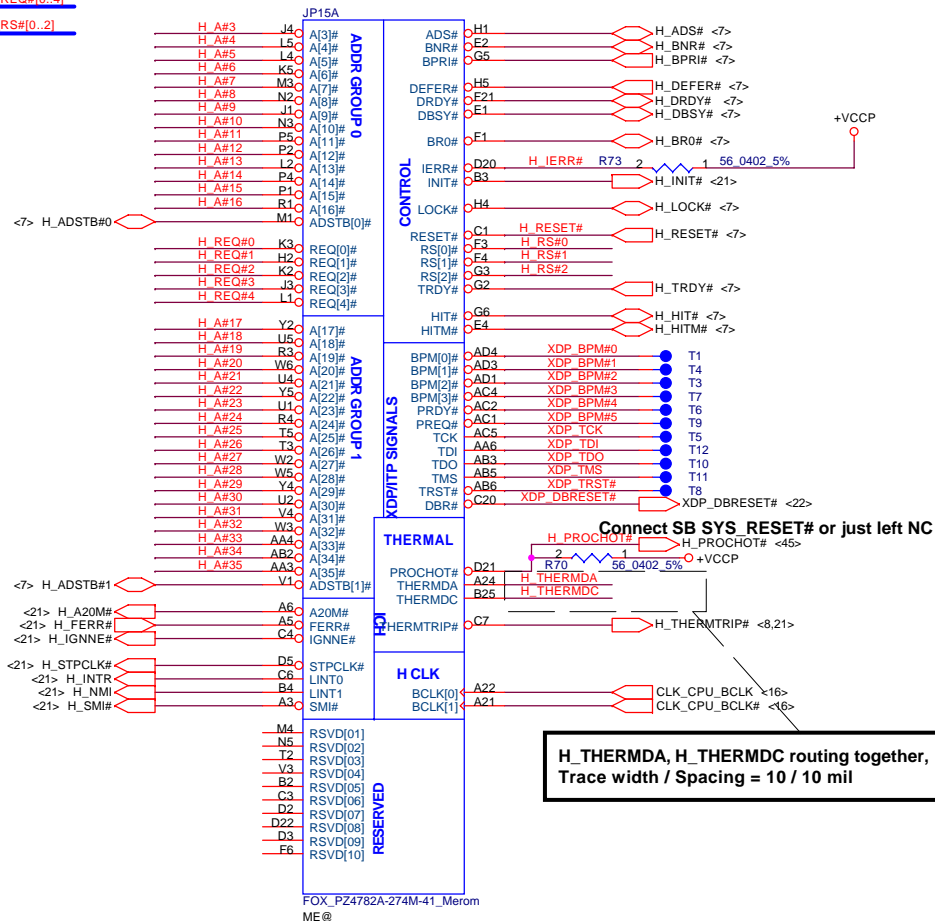
EC SM Bus2 address

Device	Address
GMT-781	1001 100X b
NVIDIA NB8X	

ICH8M SM Bus address

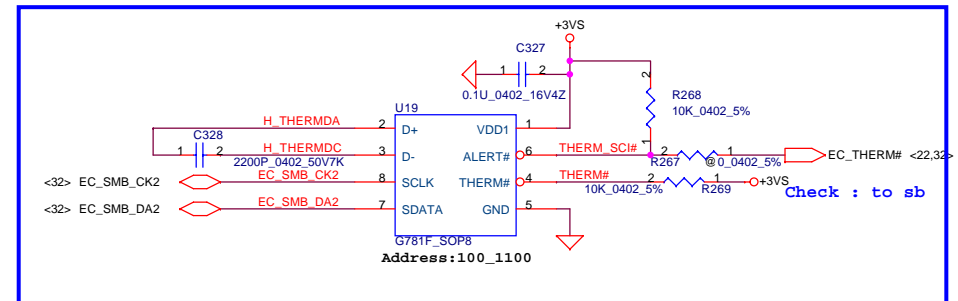
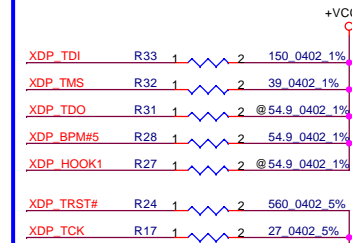
Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

<7> H\_A# [3..35]  H\_A# [3..35]  
 <7> H\_REQ# [0..4]  H\_REQ# [0..4]  
 <7> H\_RS# [0..2]  H\_RS# [0..2]

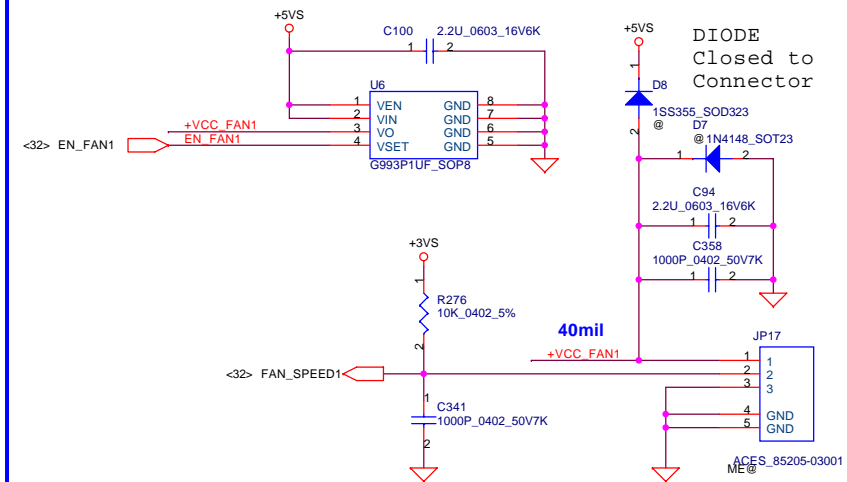


Place close to CPU within 500mil

## XDP Reserve

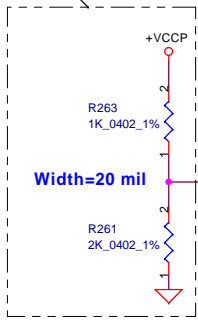


## FAN1 Conn

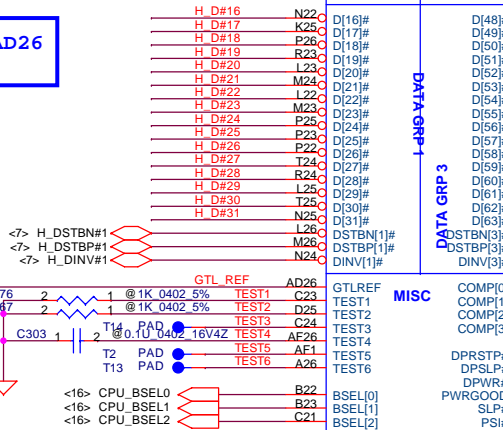


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Close to CPU pin AD26  
within 500mils.



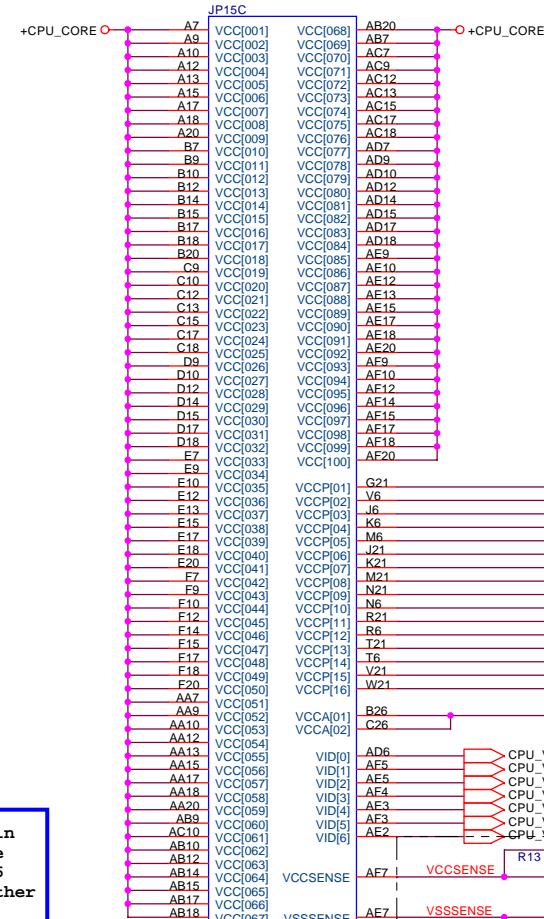
Width=20 mil



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor placed within  
0.5" of CPU pin. Trace  
should be at least 25  
mils away from any other  
toggling signal.  
COMP[0,2] trace width is  
18 mils. COMP[1,3] trace  
width is 4 mils.



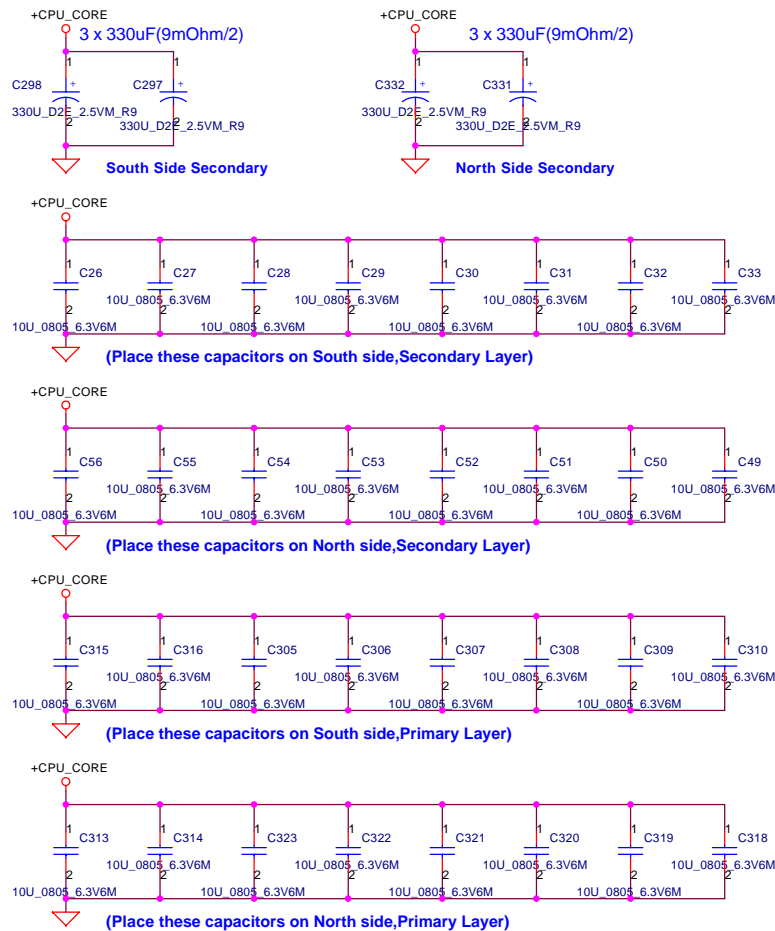
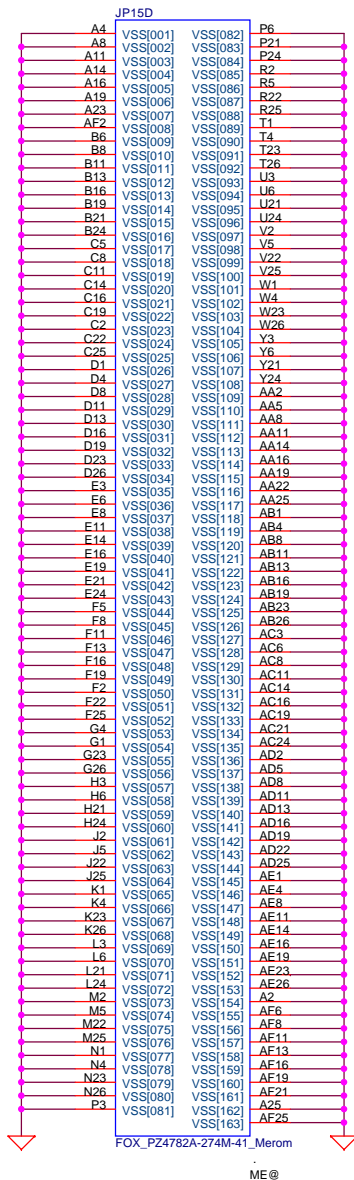
Place this cap more close to  
B26/C26 rather than 10UF

20mils

Length match within 25 mils.  
The trace width/space/other is  
20/7/25.

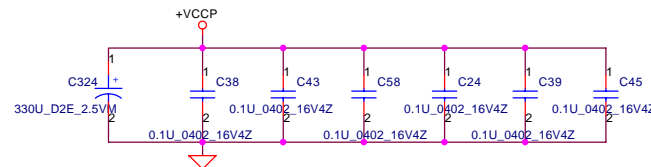
Close to CPU pin  
within 500mils.

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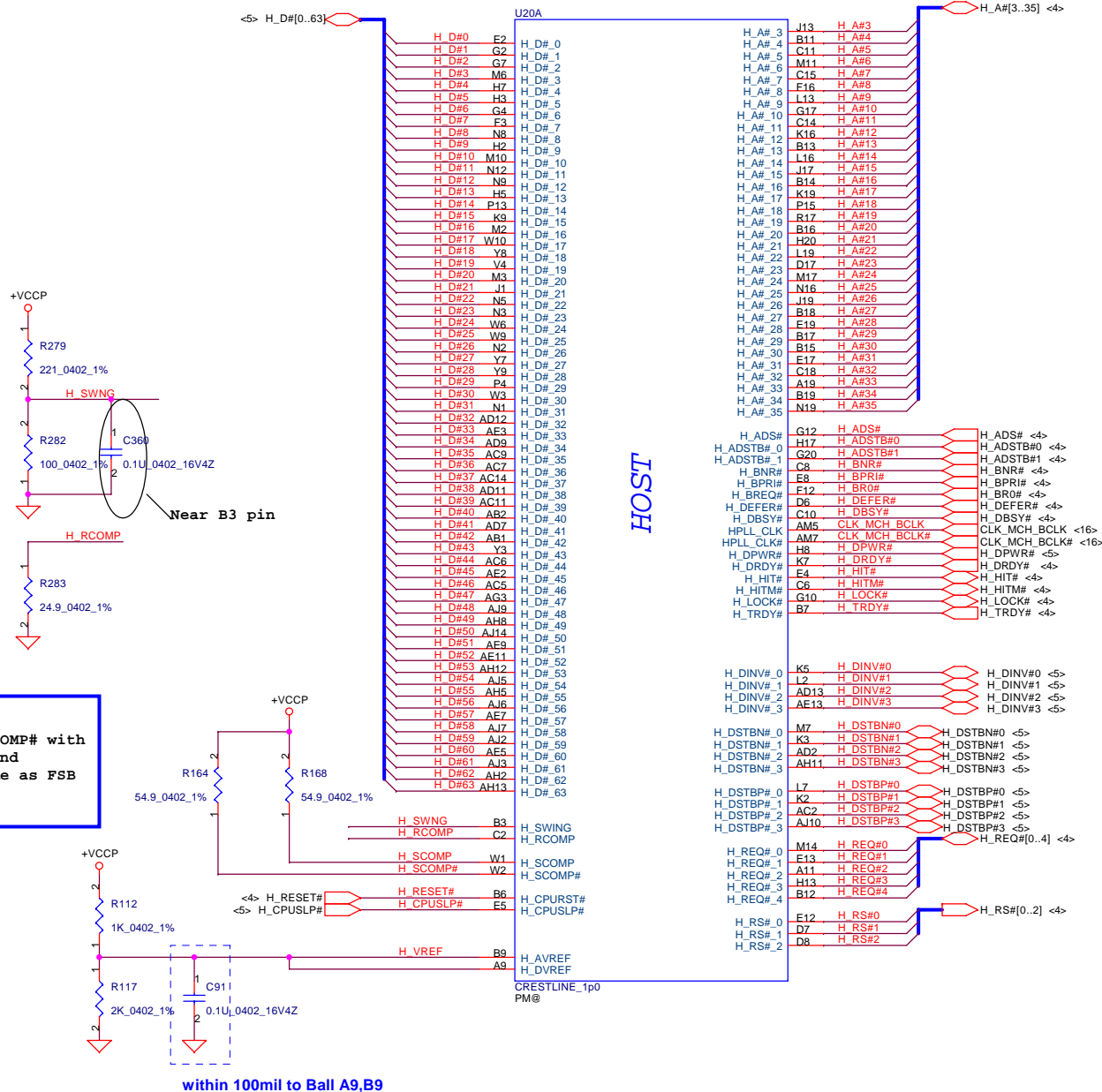


9/25 10U checked. OK for use!

+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



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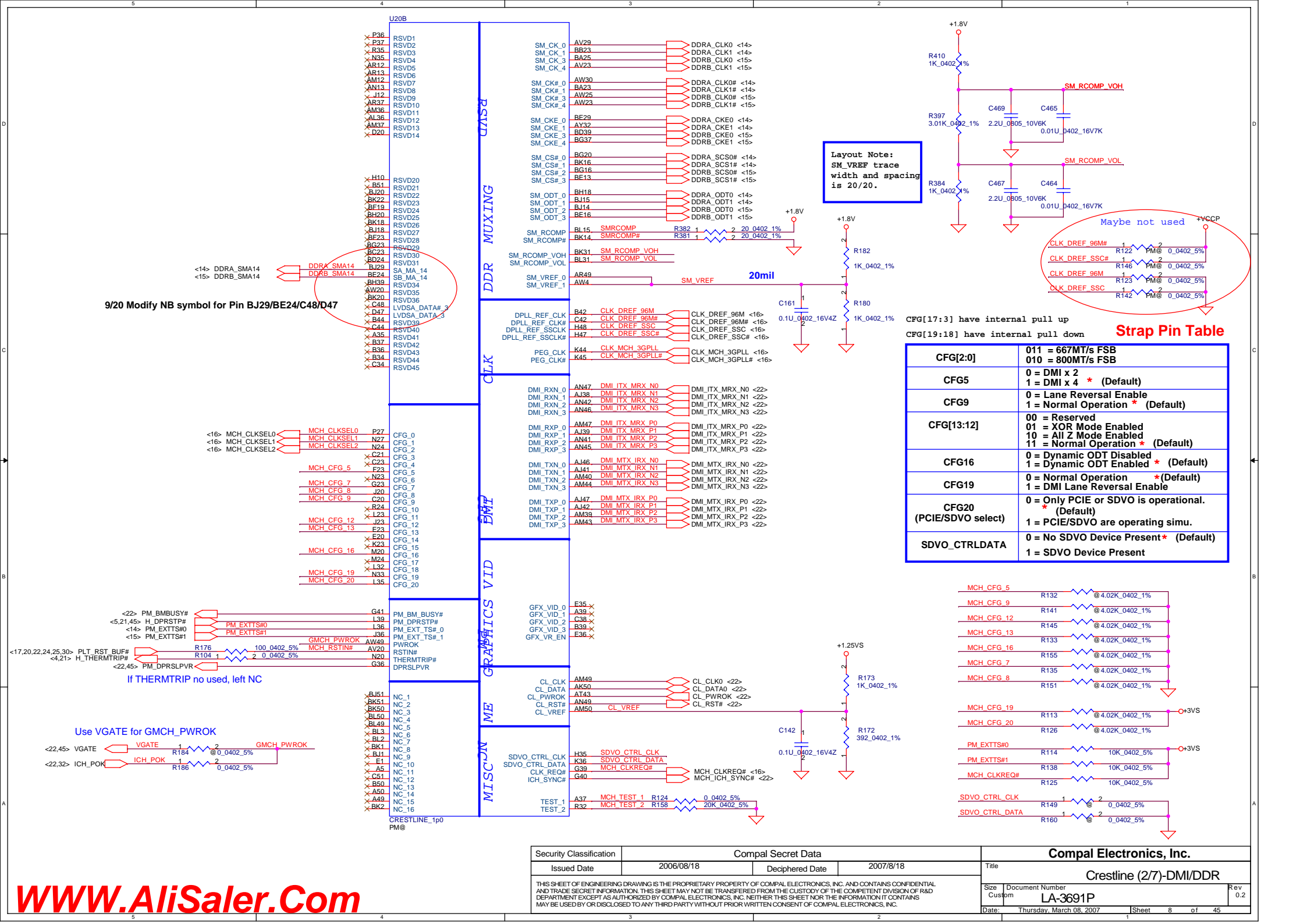
layout note:  
Route H\_SCOMP and H\_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:  
H\_RCOMP / H\_VREF / H\_SWNG  
trace width and spacing is 10/20

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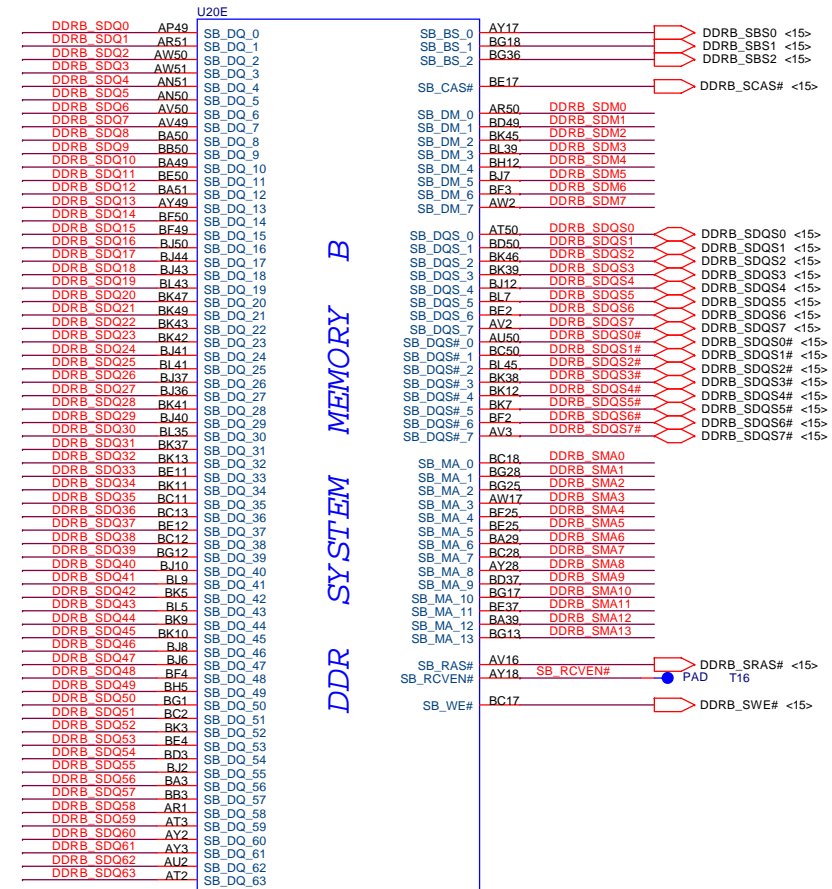
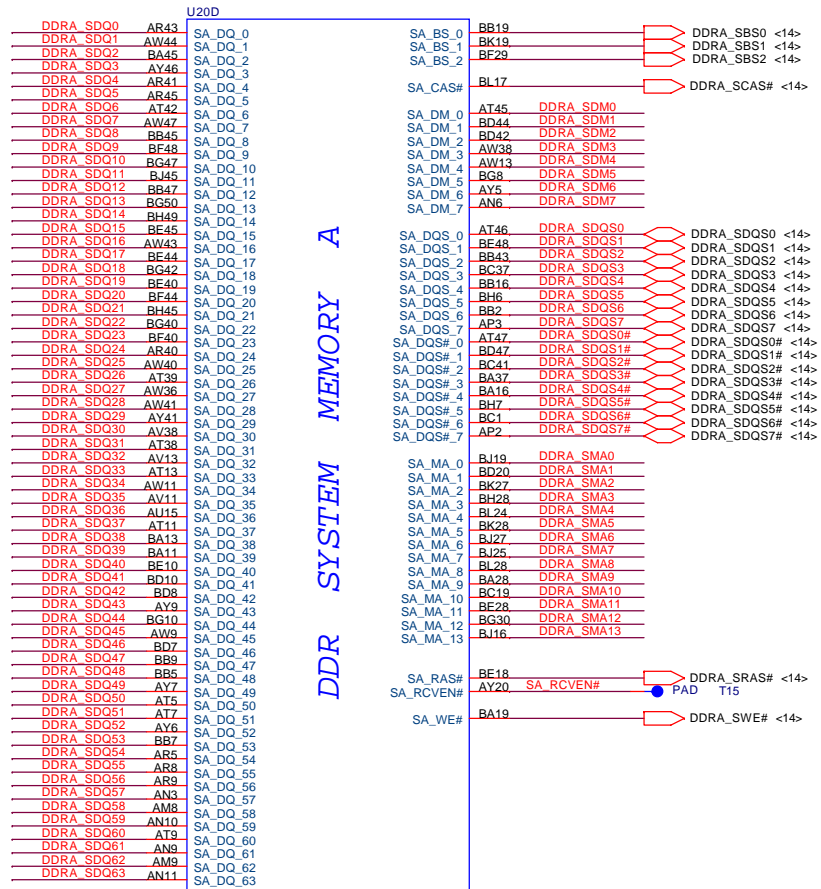






<14> DDRA\_SDQ[0..63] <--> DDRA\_SDQ[0..63]  
<14> DDRA\_SDM[0..7] <--> DDRA\_SDM[0..7]  
<14> DDRA\_SMA[0..13] <--> DDRA\_SMA[0..13]

<15> DDRB\_SDQ[0..63] <--> DDRB\_SDQ[0..63]  
<15> DDRB\_SDM[0..7] <--> DDRB\_SDM[0..7]  
<15> DDRB\_SMA[0..13] <--> DDRB\_SMA[0..13]



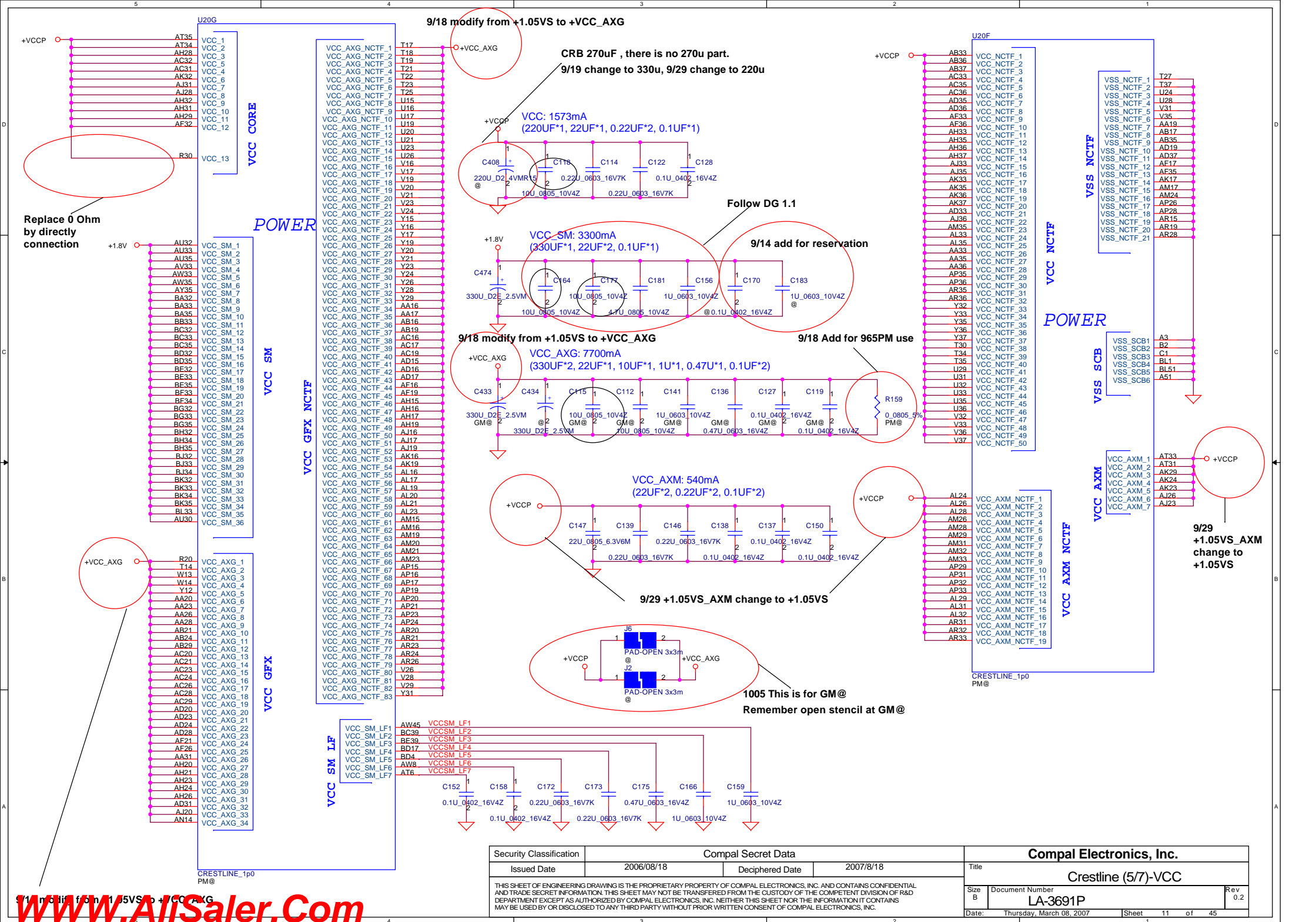
CRESTLINE\_1p0  
PM@

CRESTLINE\_1p0  
PM@

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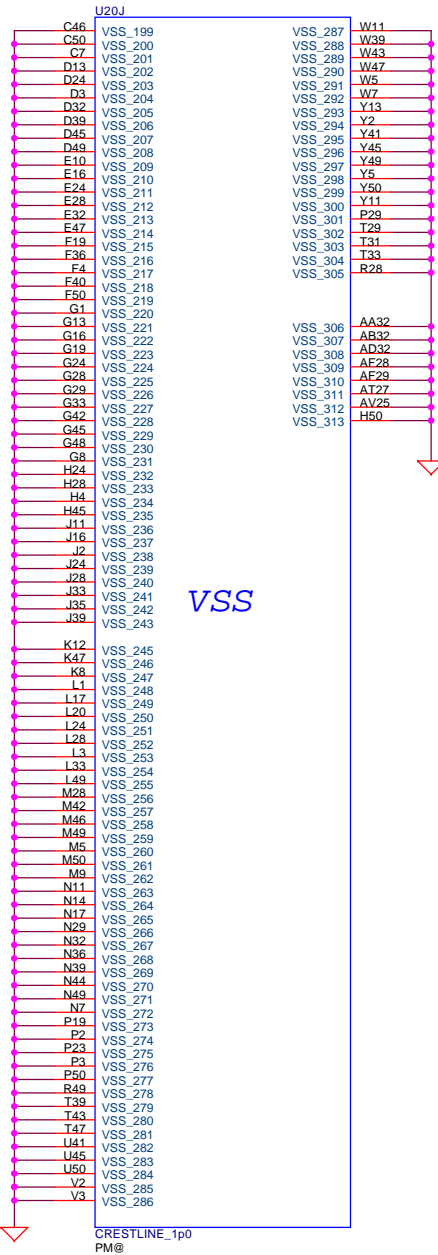
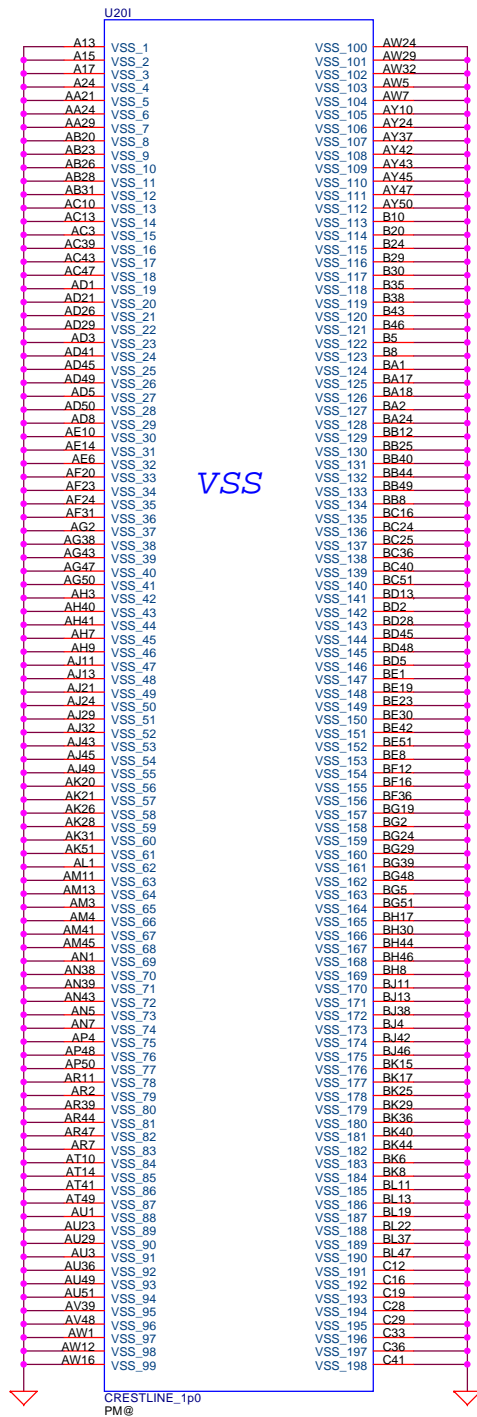




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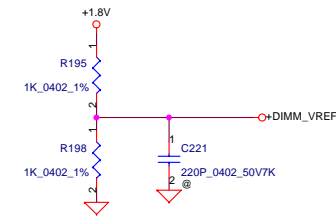
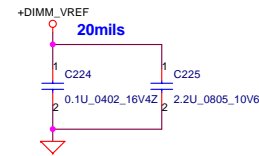
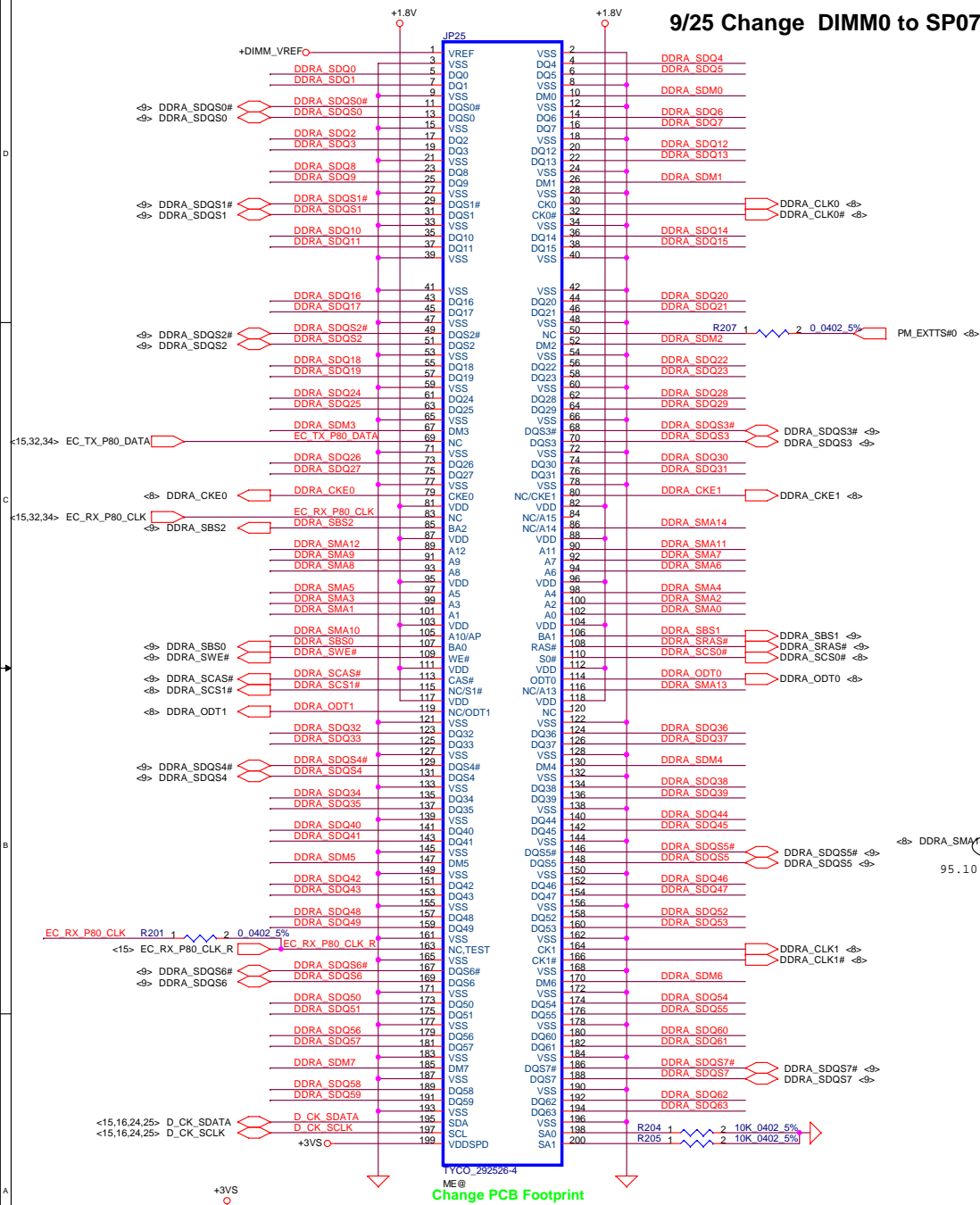




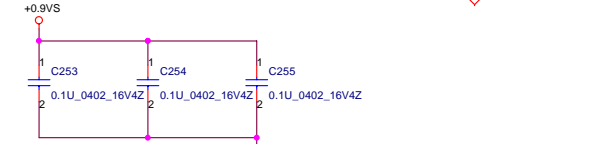
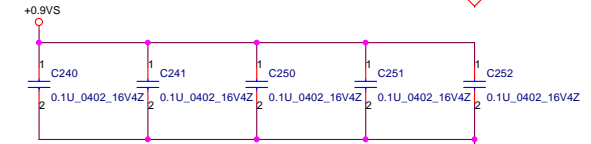
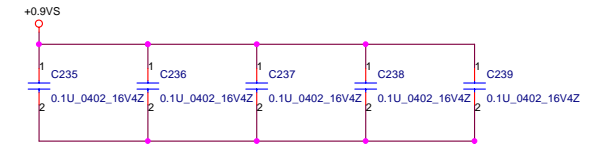
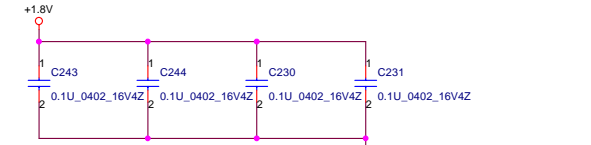
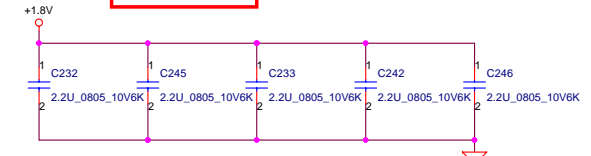


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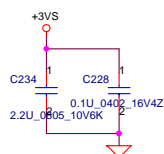
**9/25 Change DIMM0 to SP070004Z00 (HBL50)**



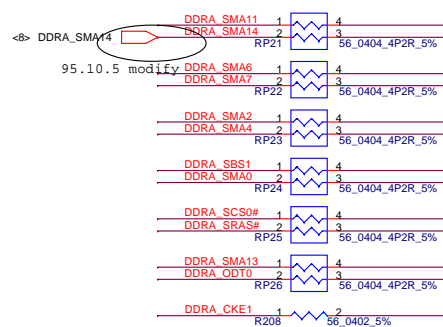
**Layout Note:**  
Place near JP35



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



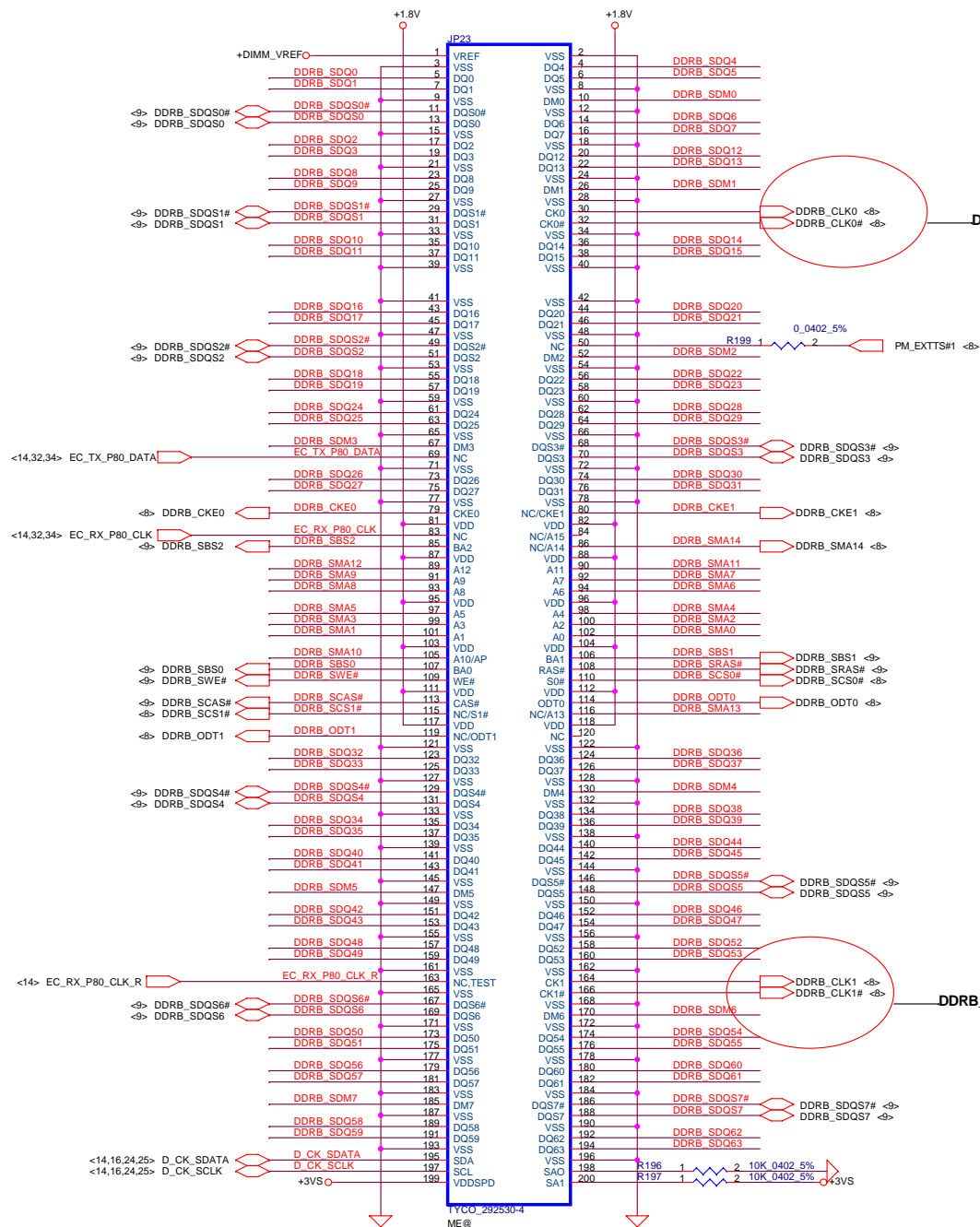
**DIMM0 STD H:5.2mm (BOT)**



**Layout Note:**  
Place these resistor  
closely JP35,all  
trace length Max-1.5

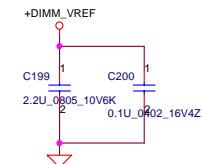
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# 9/25 Change DIMM1 to SP070006F00

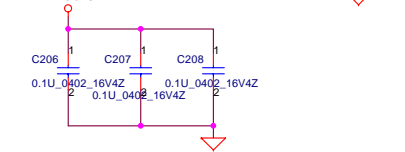
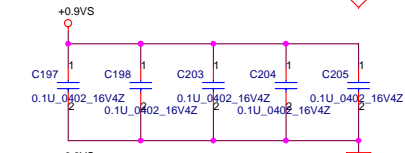
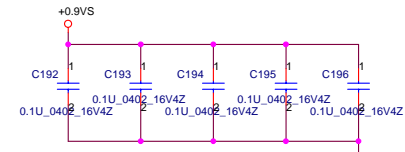
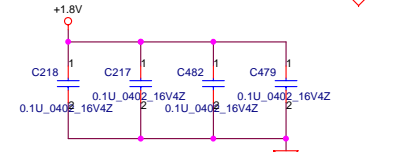
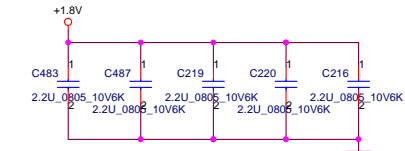


DIMM1 STD H:9.2mm (BOT)

DDR\_B\_SMA[0..13] → DDRB\_SMA[0..13]  
 DDR\_B\_SQ[0..63] → DDRB\_SQ[0..63]  
 DDR\_B\_SDM[0..7] → DDRB\_SDM[0..7]



Layout Note:  
Place near JP34



Layout Note:  
Place these resistor  
closely JP35, all  
trace length Max=1.5"

Layout Note:  
Place one cap close to every 2 pullup  
resistors terminated to +0.9VS

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Routing the trace at least 10mil

Routing the trace at least 10mil

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Routing the trace at least 10mil

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Routing the trace at least 10mil

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Routing the trace at least 10mil

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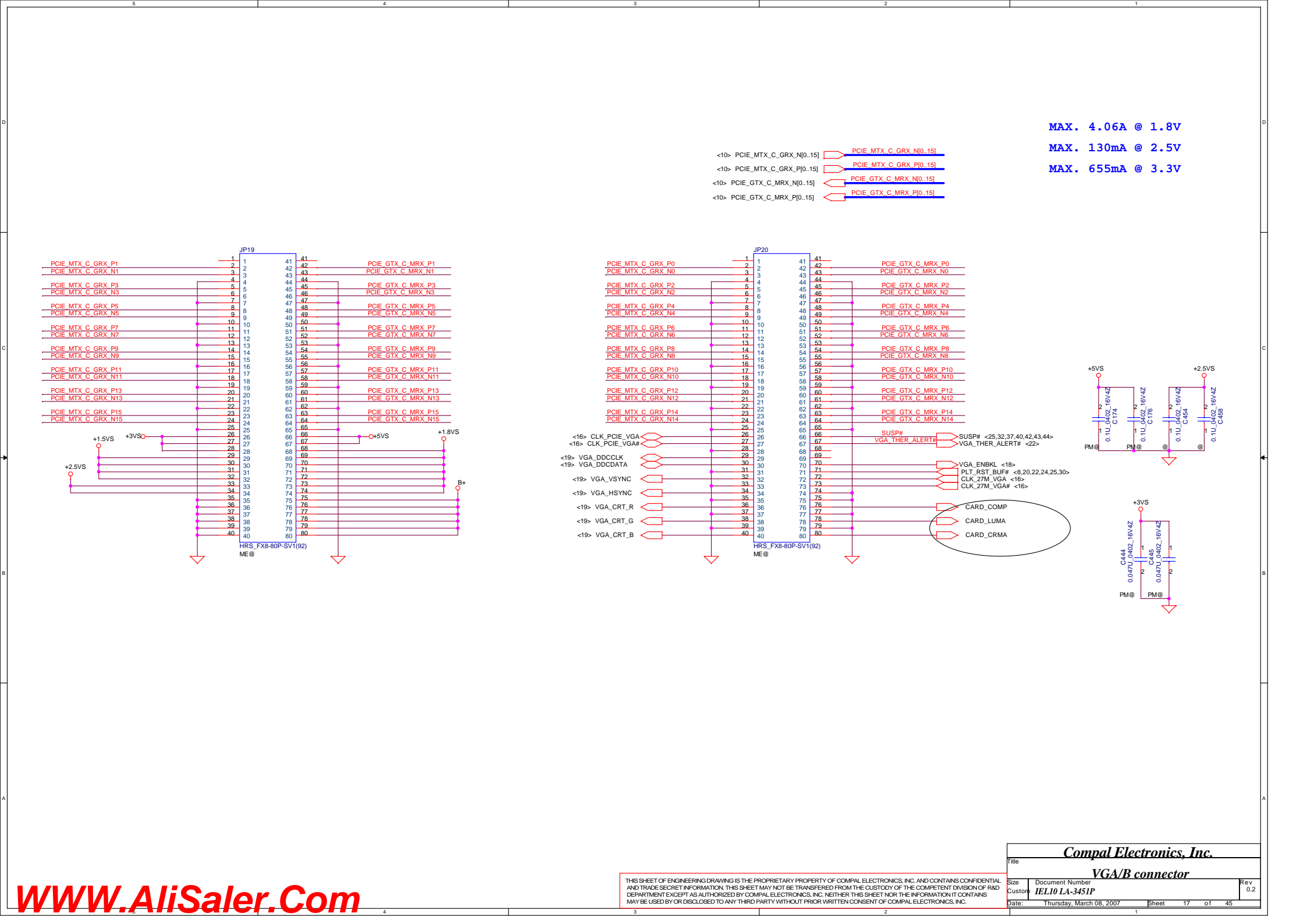


Routing the trace at least 10mil

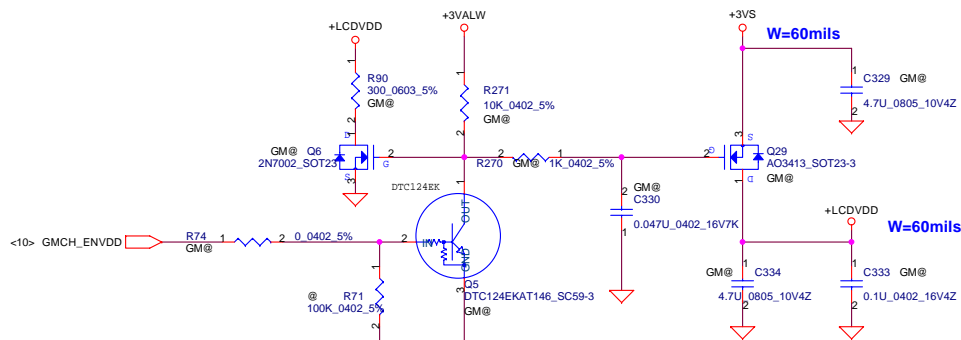
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Routing the trace at least 10mil

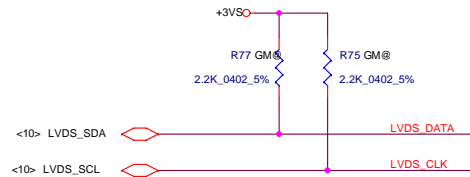
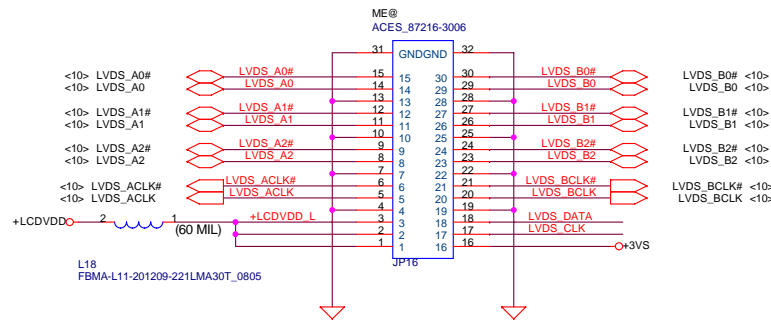
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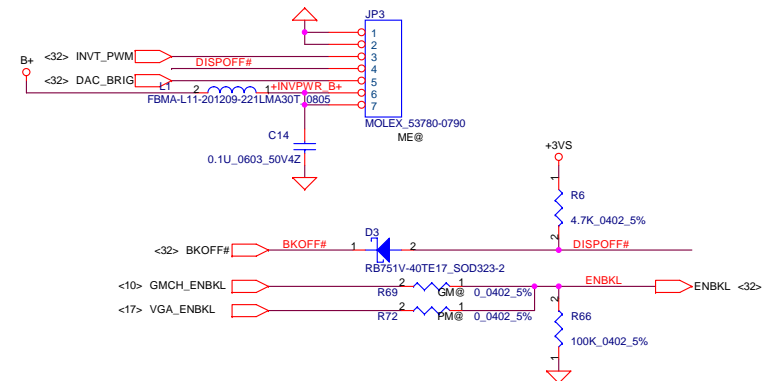
## LCD POWER CIRCUIT



## LCD/PANEL BD. Conn.



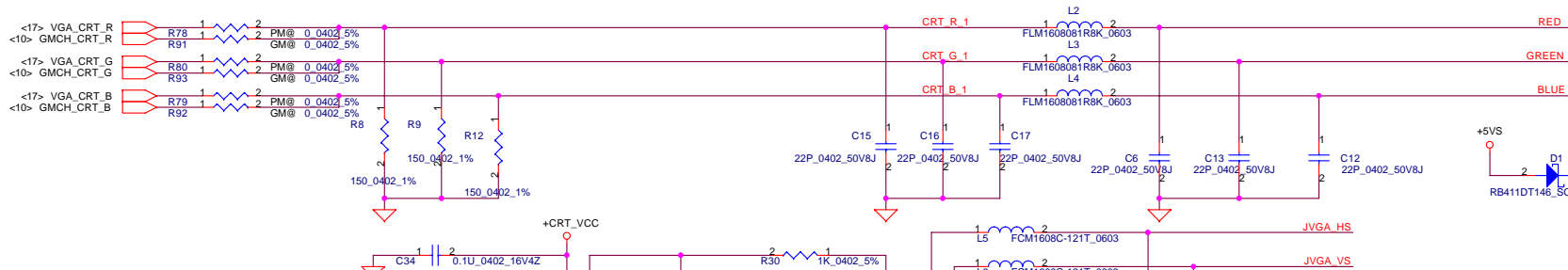
## INVERTER Conn.



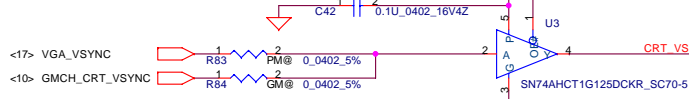
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# CRT Connector

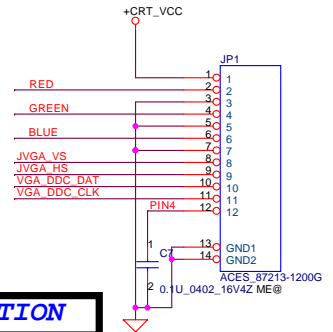
Place closed to chipset



Place closed to chipset



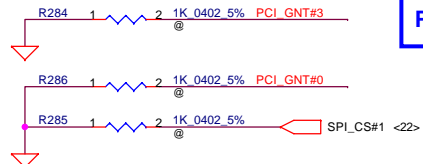
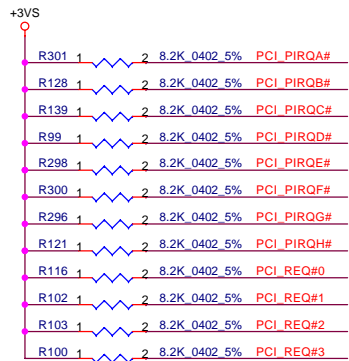
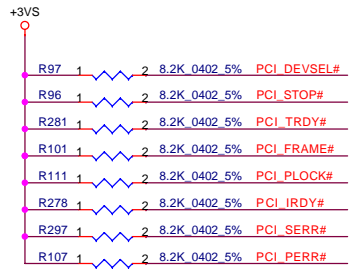
Update Footprint



## PIN ASSIGNMENT

PIN	D-SUB	FUNCTION
1	9	+CRT_VCC
2	1	RED
3	6	GND
4	2	GREEN
5	7	GND
6	3	BLUE
7	8	GND
8	14	VSYNC
	10	GND
9	13	HSYNC
	11	SENSE
10	12	SM_DAT
11	15	SM_CLK
12	4	PIN4

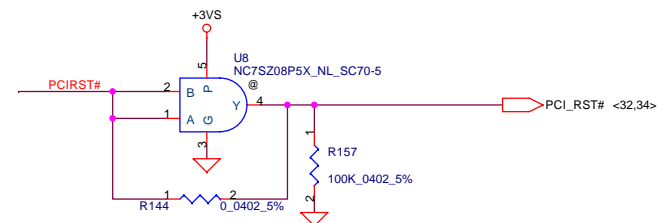
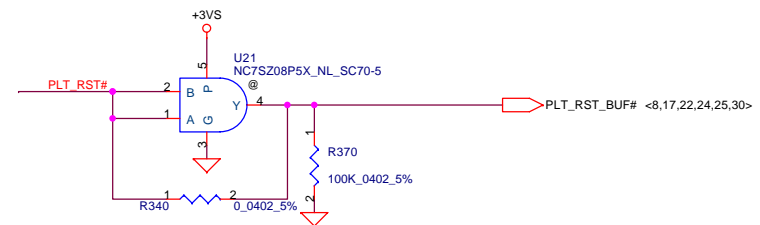
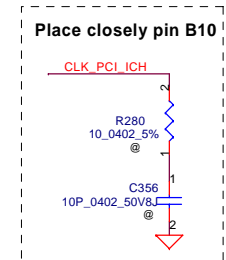
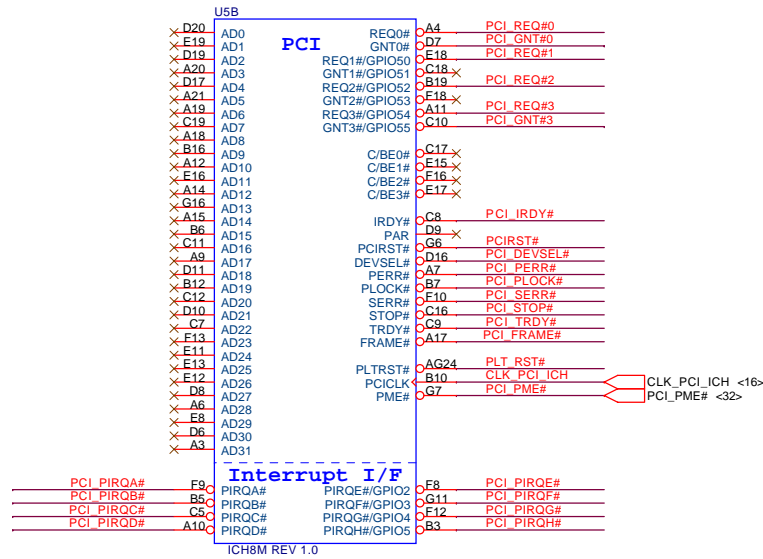
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				Date: Thursday, March 06, 2007	Sheet 19 of 45



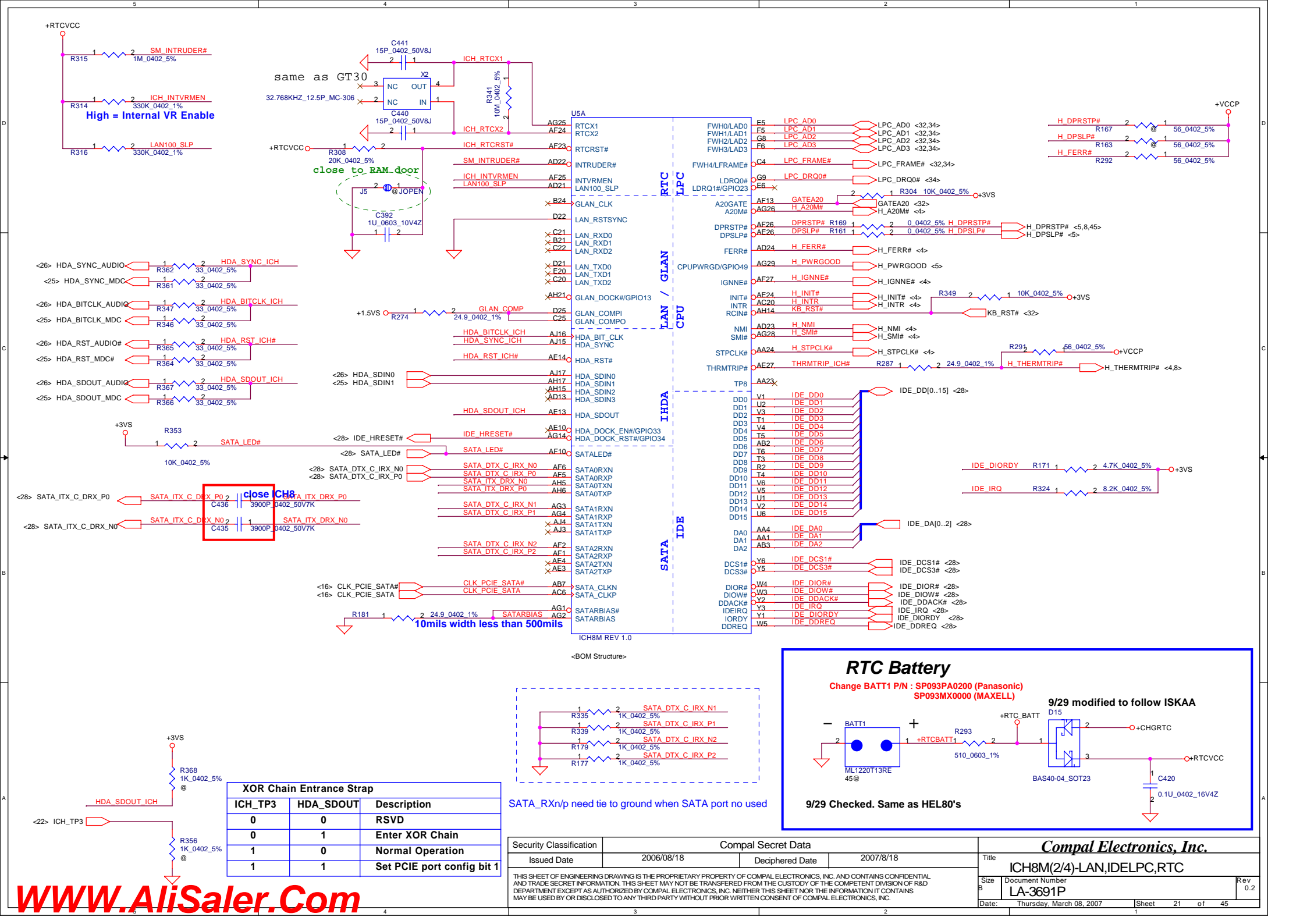
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

10/17 : Change P/N from SA000010G00 to SA00001JU10  
 10/17 : FootPrint : SA000010G00  
 BOM : SA00001JU10



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Size		Document Number		Rev	
		LA-3691P		0.2	
Date		Thursday, March 08, 2007		Sheet 20 of 45	



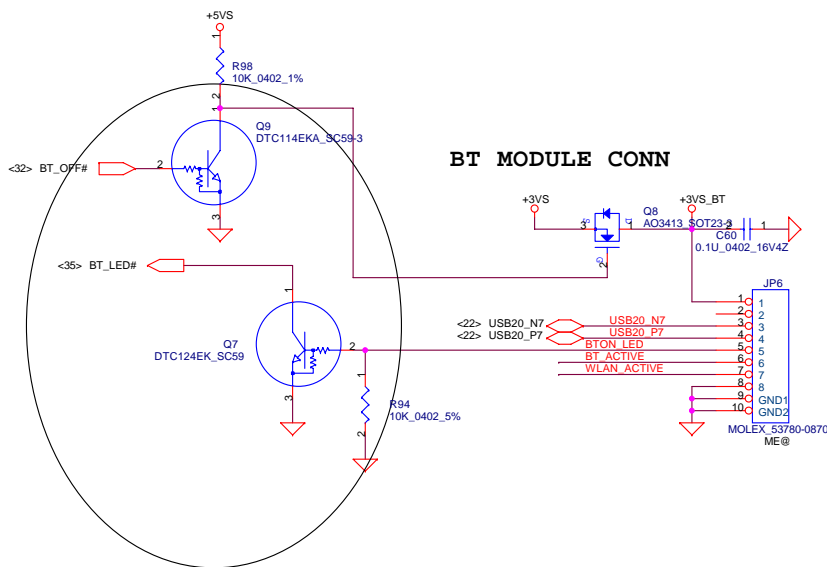
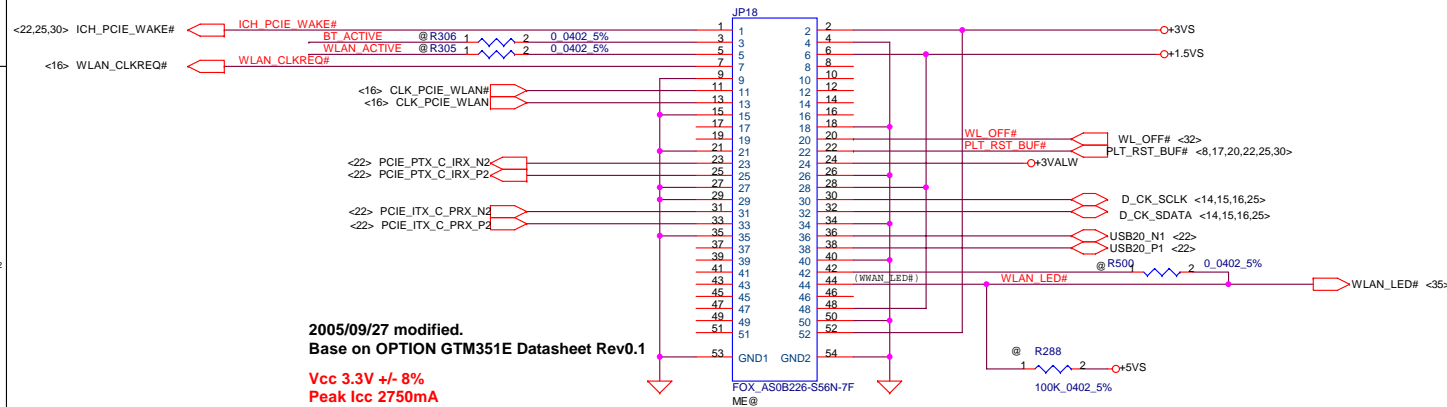
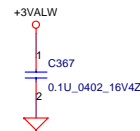
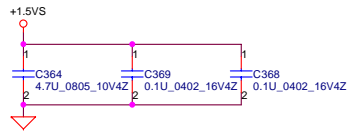
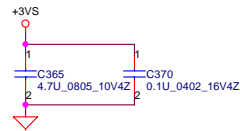






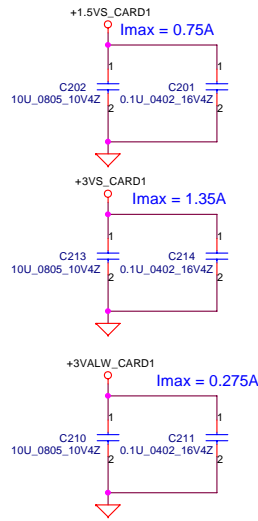
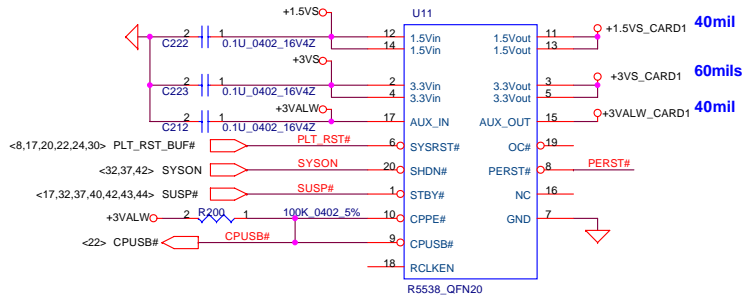
# Mini-Express Card for 3G Or TV Tuner

## Mini-Express Card for WLAN

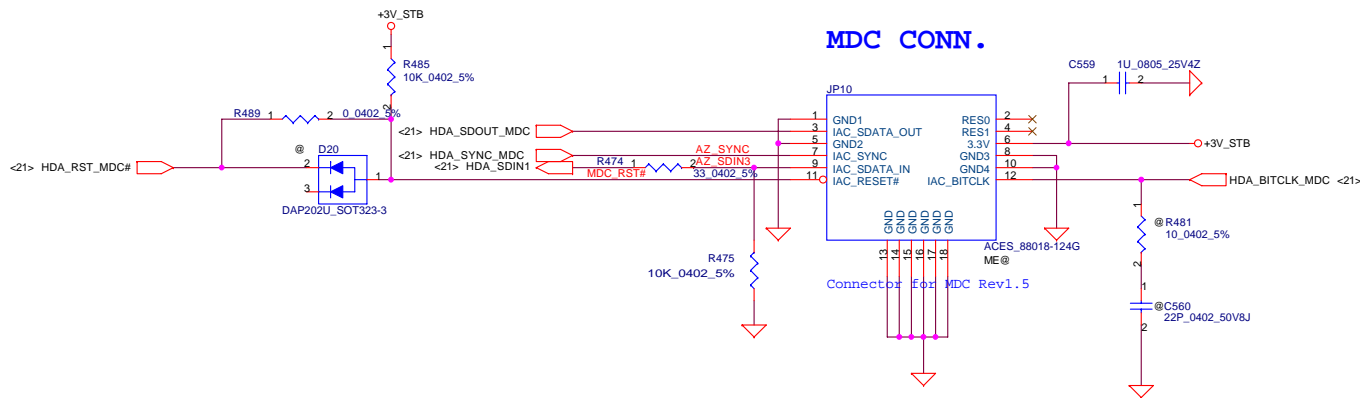
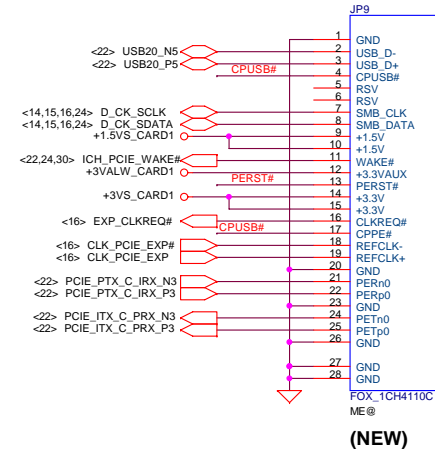


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# Express Card Power Switch



# New Card Socket (Left/TOP)

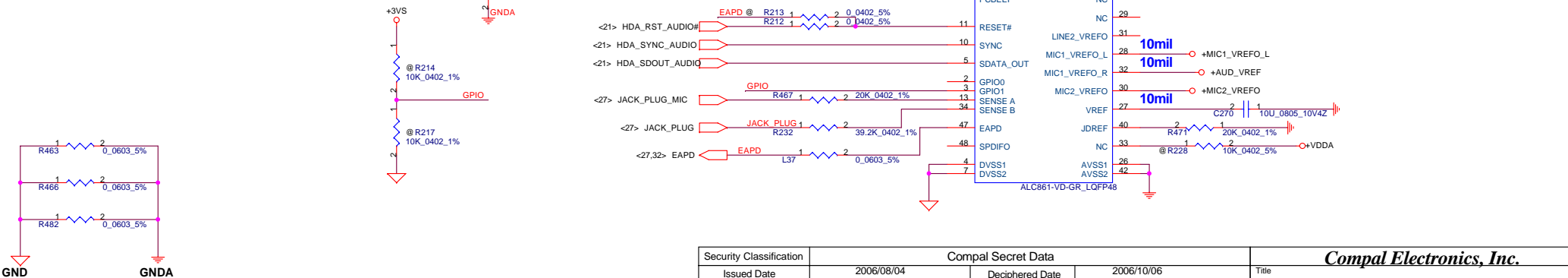
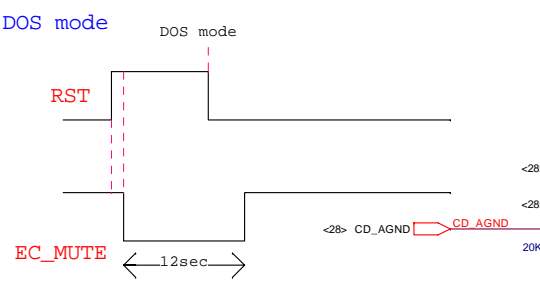
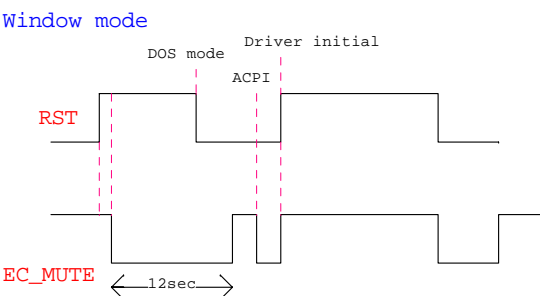
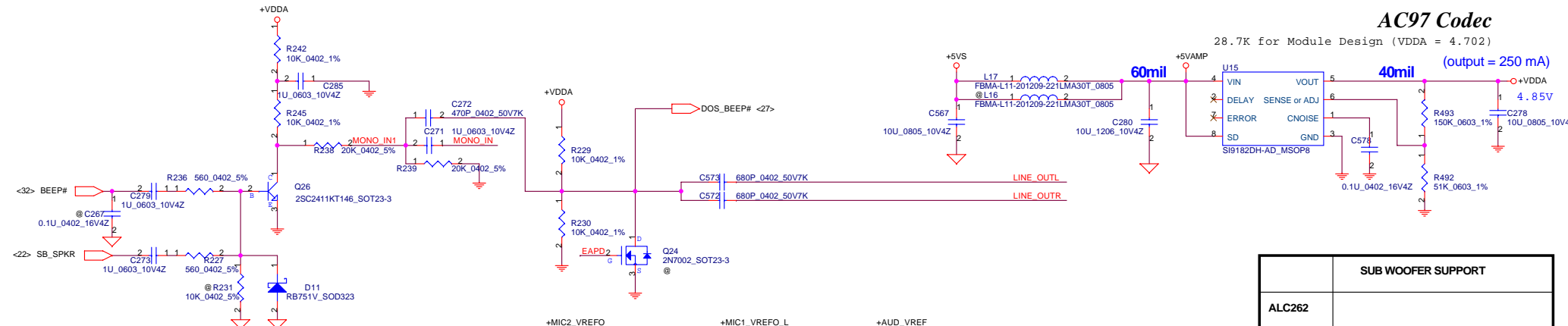


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				Size B	Document Number
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# AC97 Codec

28.7K for Module Design (VDDA = 4.702)

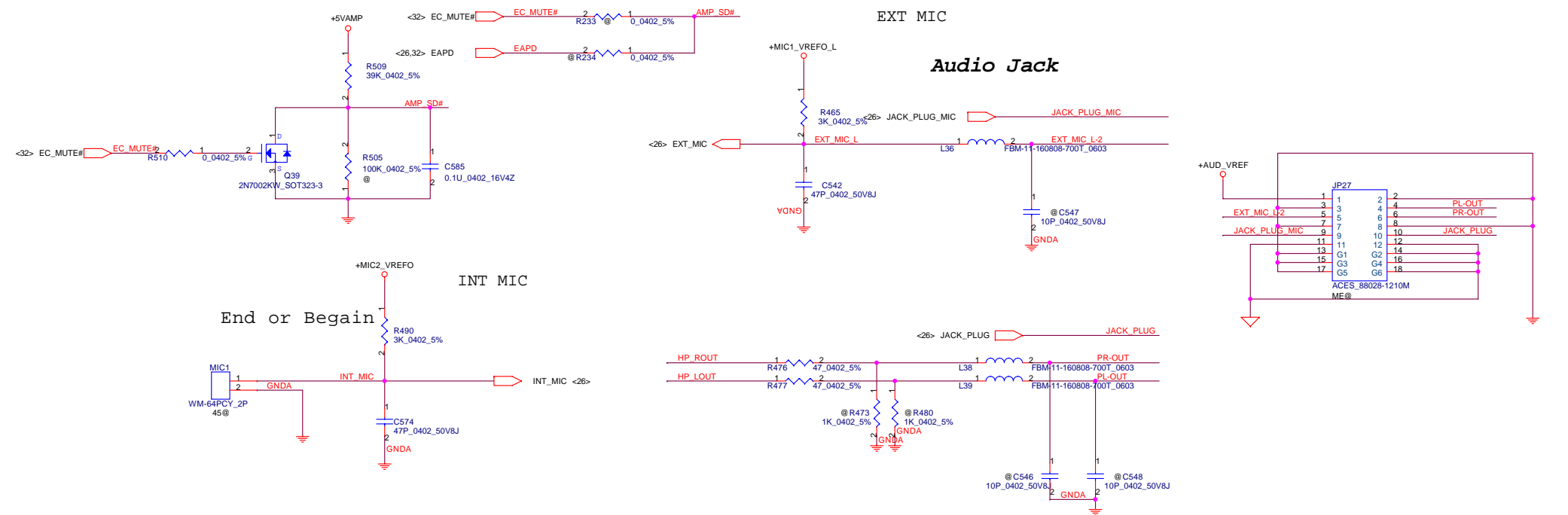
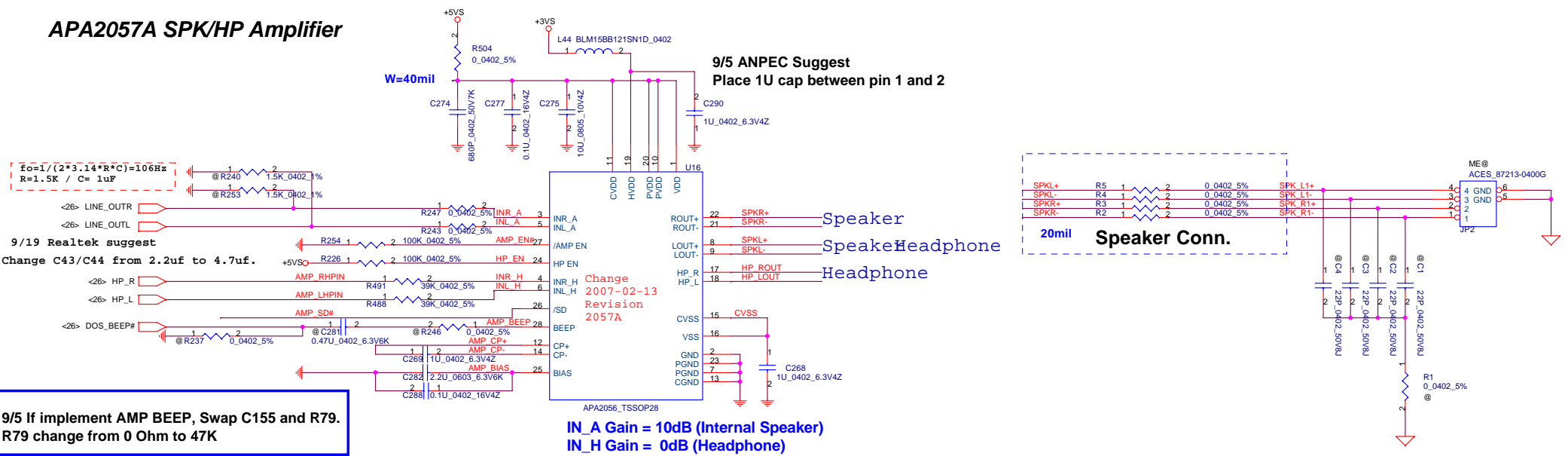
(output = 250 mA)



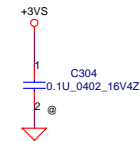
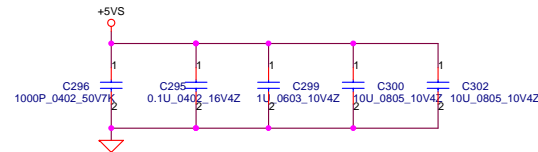
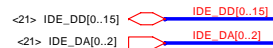
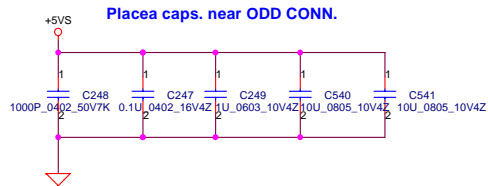
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				Custom	IEL10 LA-3451P
				Date	Thursday, March 08, 2007
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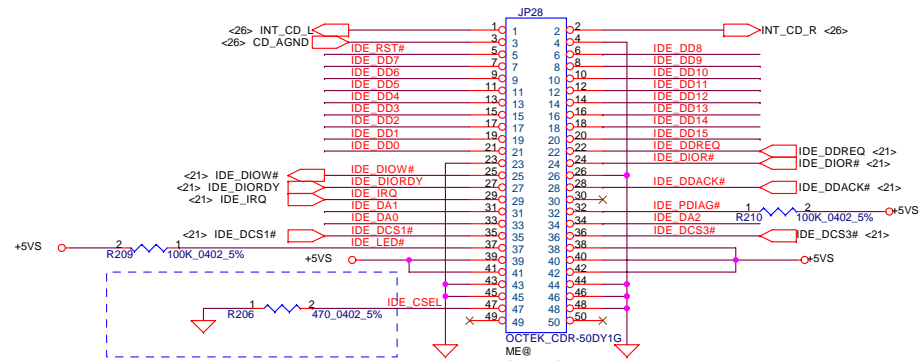
## APA2057A SPK/HP Amplifier



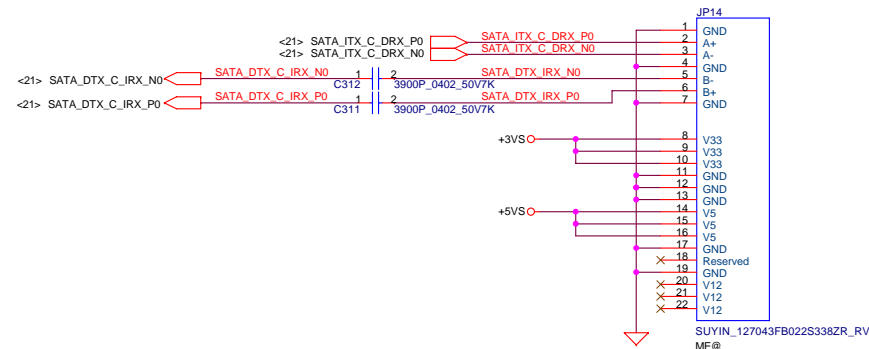
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/08/05	Deciphered Date	2007/08/05	Title	AMP/VR/Audio Jack/MIC	
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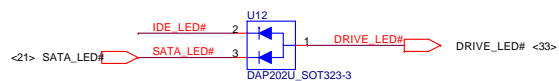
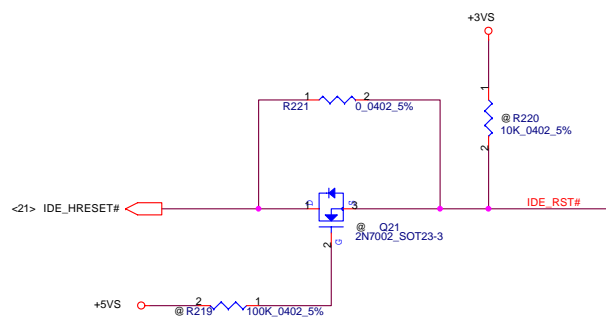
## SATA HDD Conn.



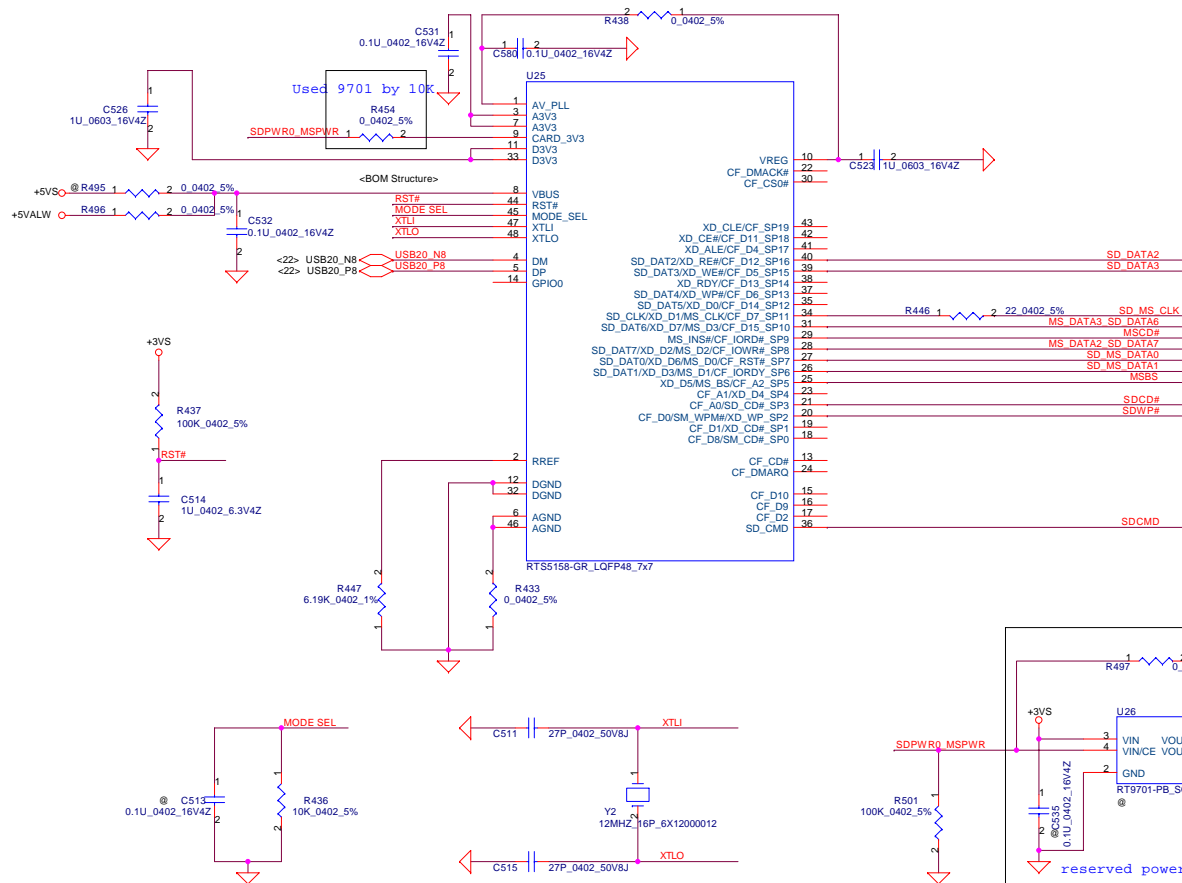
**IDE\_CSEL**  
Grounding for Master (When use SATA HDD)  
Open or High for Slaver (Normal)



**(NEW)**  
Change Library

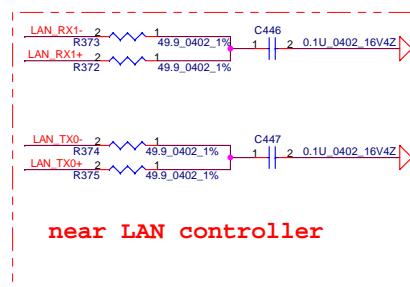


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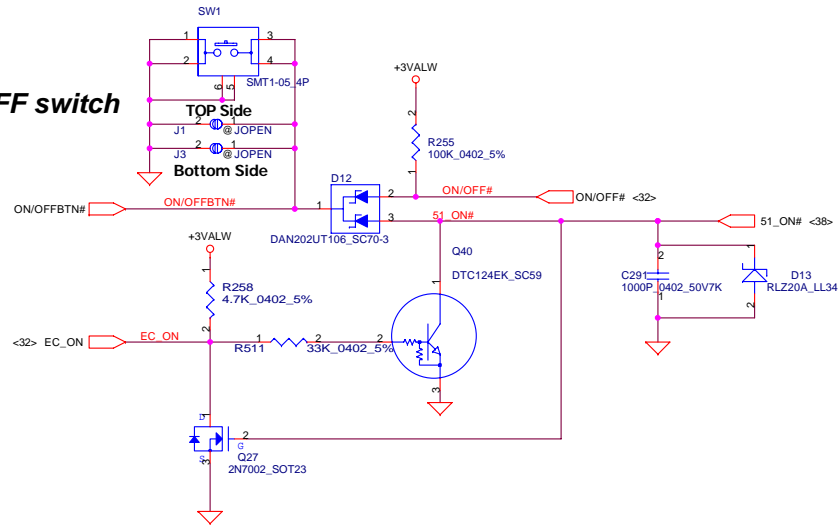


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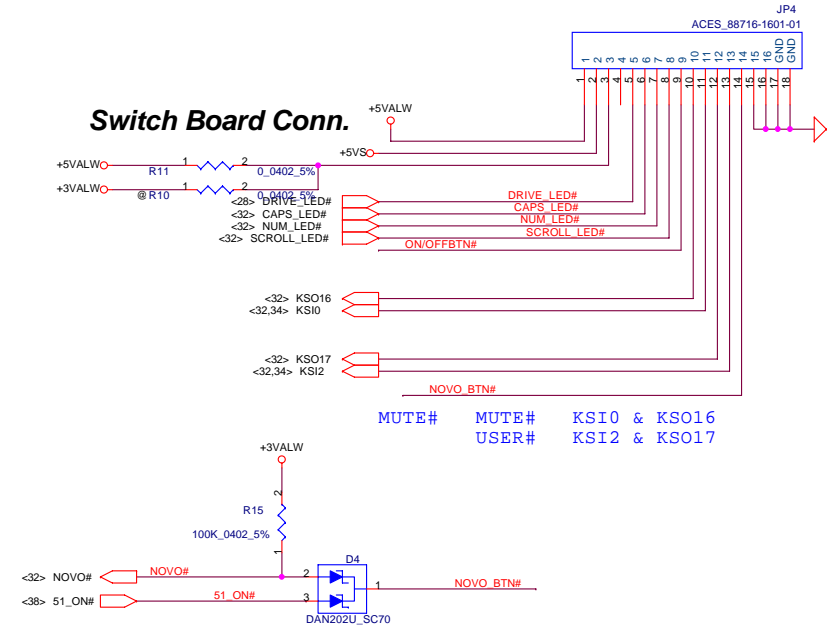


## Power Button

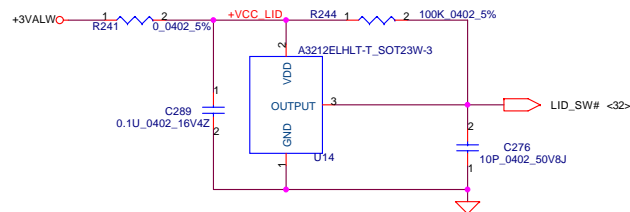
### ON/OFF switch



### Switch Board Conn.

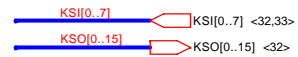


## Lid Switch

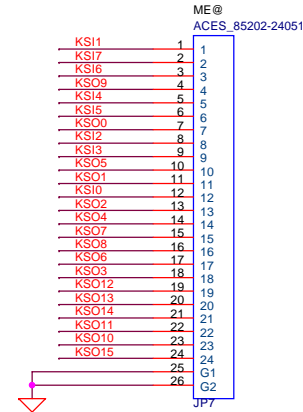
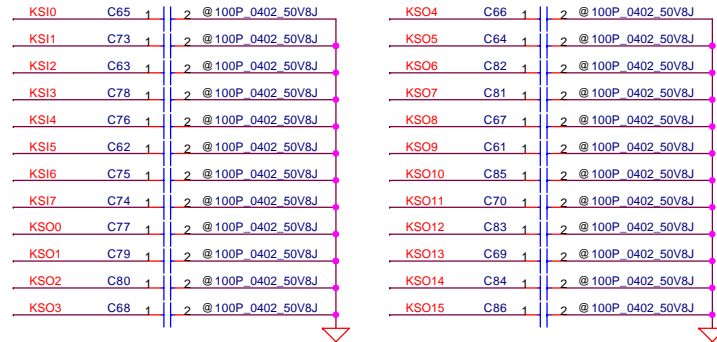


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Size	B	Document Number	LA-3691P	Rev	0.2	
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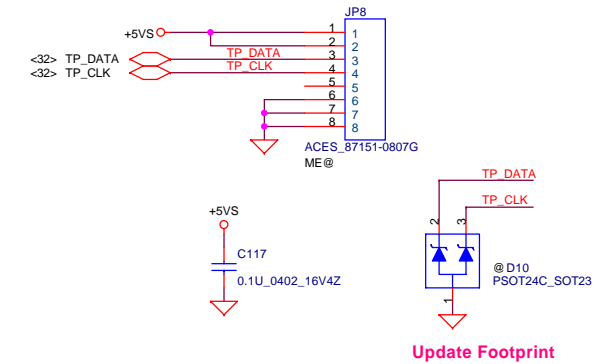
## INT\_KBD Conn.



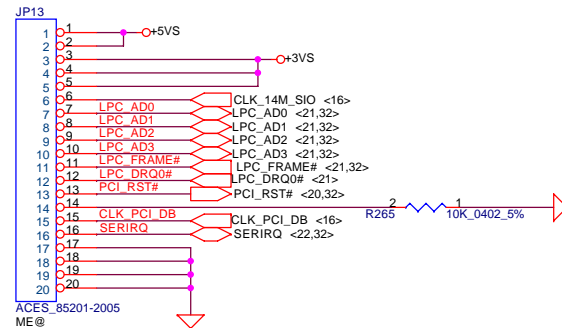
## For IHL00



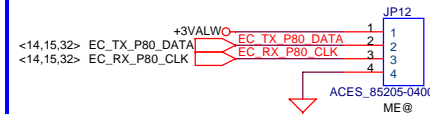
## To TP/B Conn.



## FOR LPC SIO DEBUG PORT



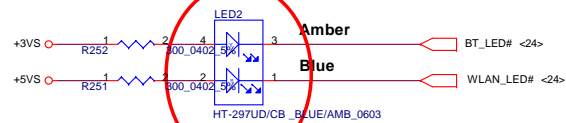
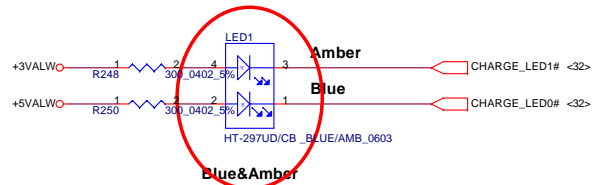
## EC DEBUG PORT



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Size	Document Number	Rev		0.2	
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Date:	Thursday, March 08, 2007	Sheet	34 of 45		

## LED

+5VALW R249 1 2 2 1 LED3  
300\_0402\_5% HT-191NB\_BLUE\_0603 PWR\_LED# <32>

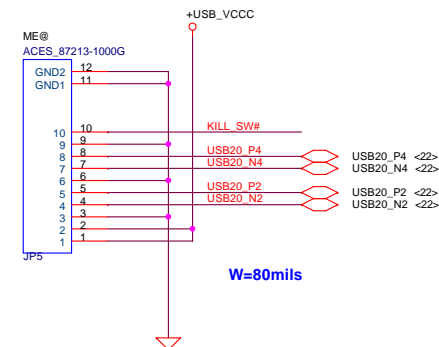
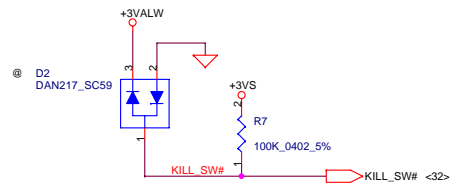


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# USB Conn.

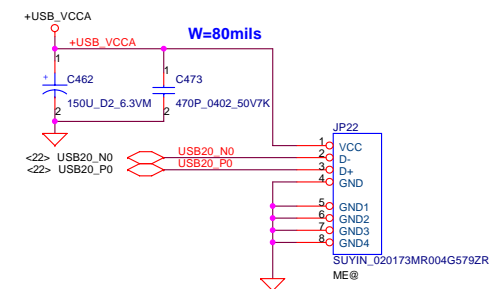
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## Kill SWITCH



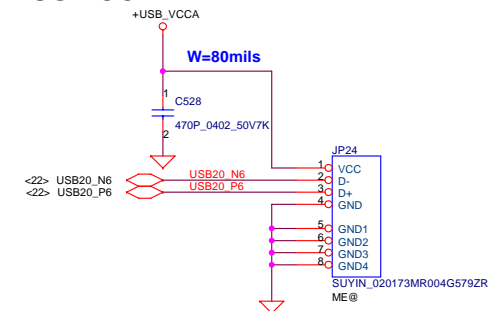
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## USB CONN. 1

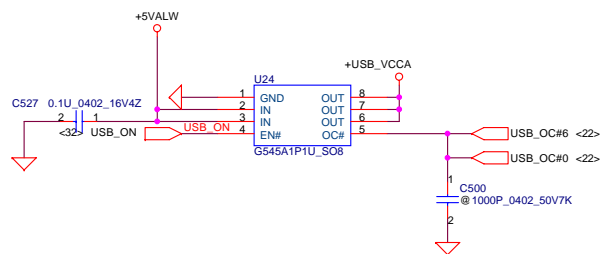
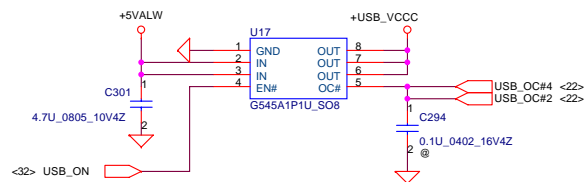


W=80mils

## USB CONN. 2

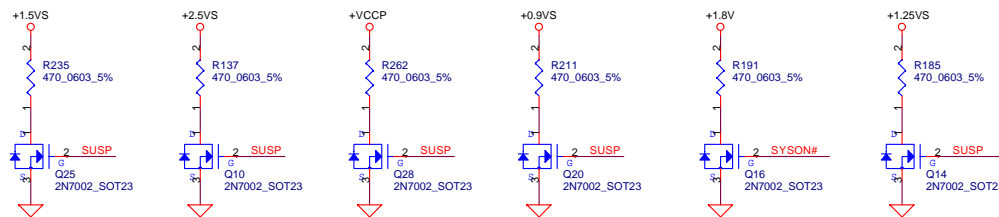
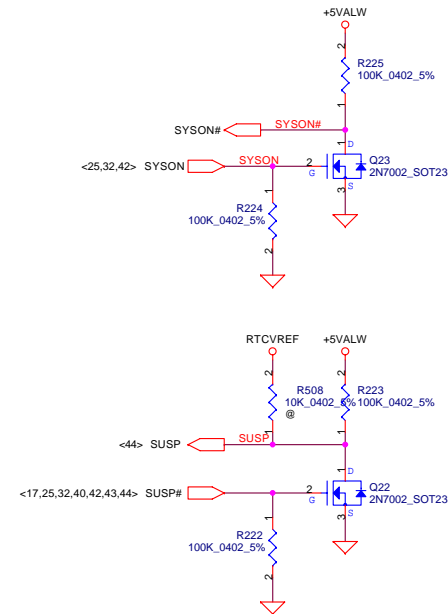
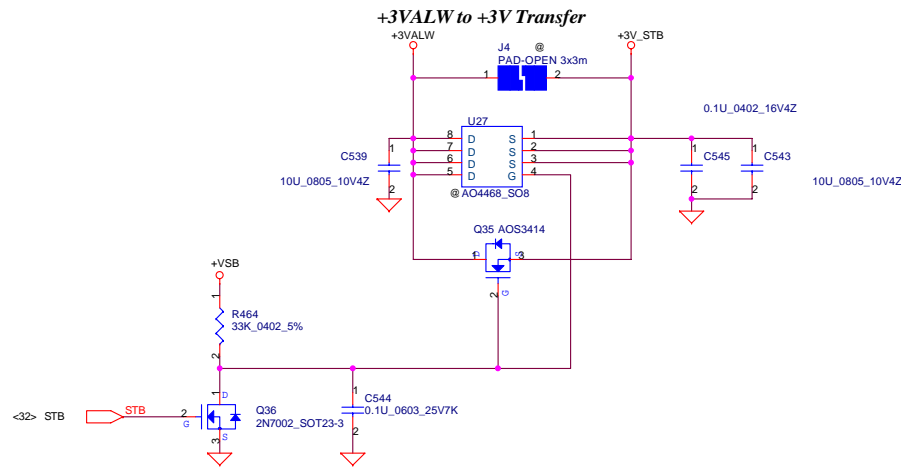
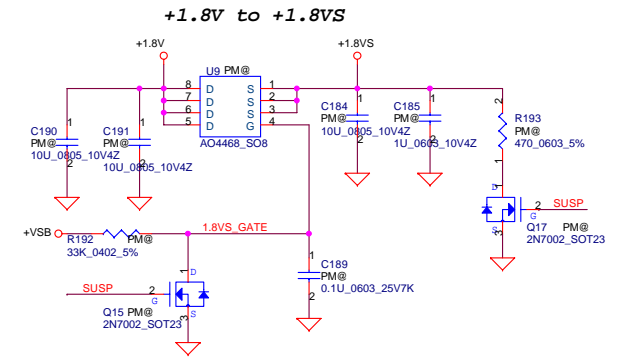
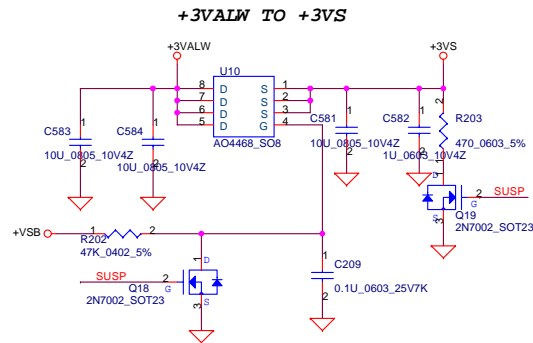
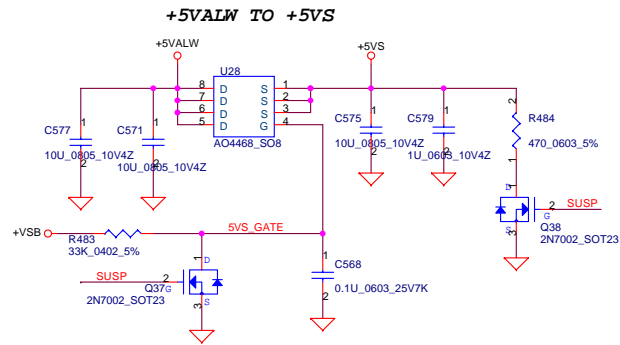


W=80mils



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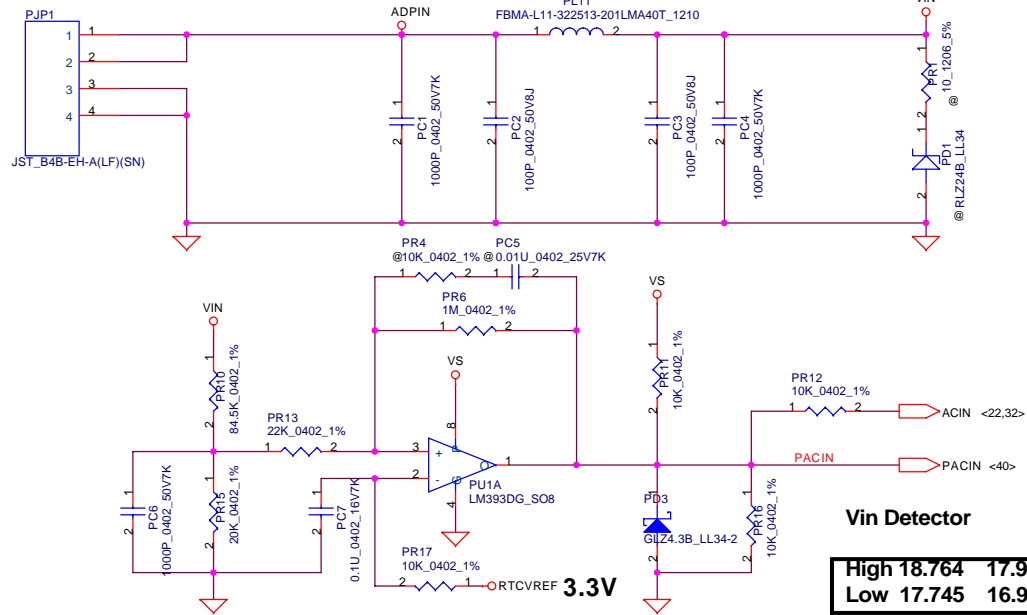


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DC Interface

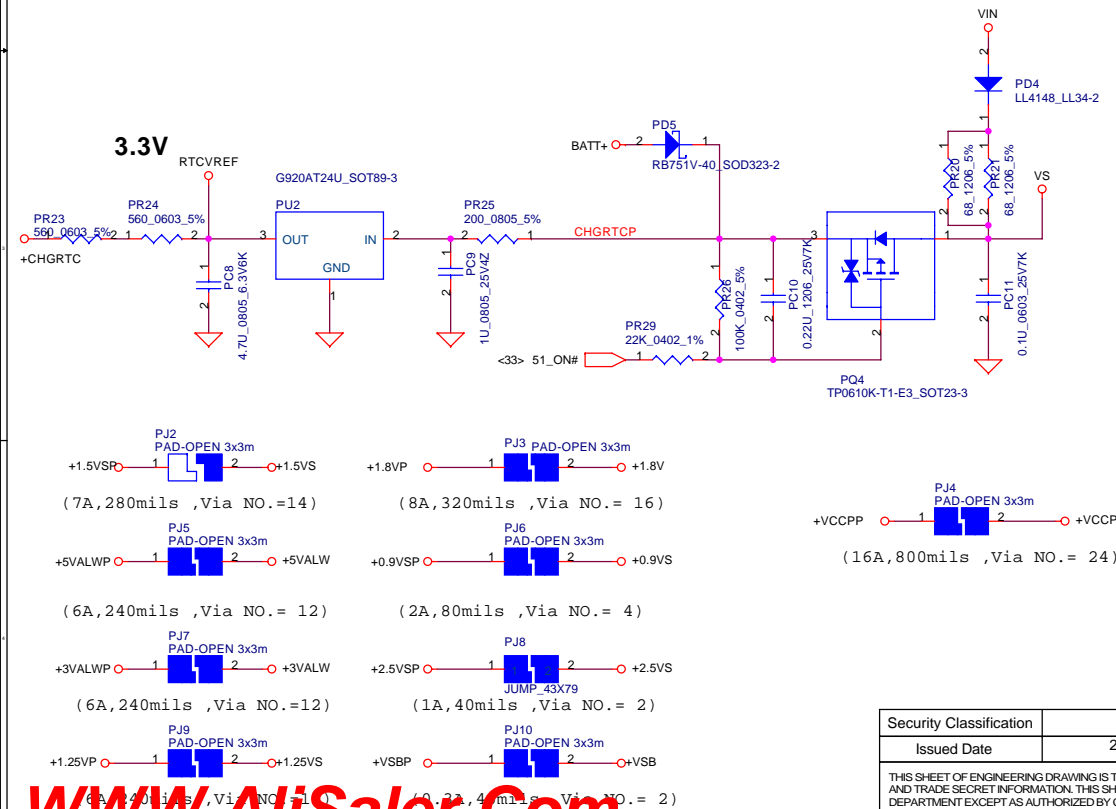
Rev 0.2

DC030005Q00



## Vin Detector

High	18.764	17.901	17.063
Low	17.745	16.9	16.03

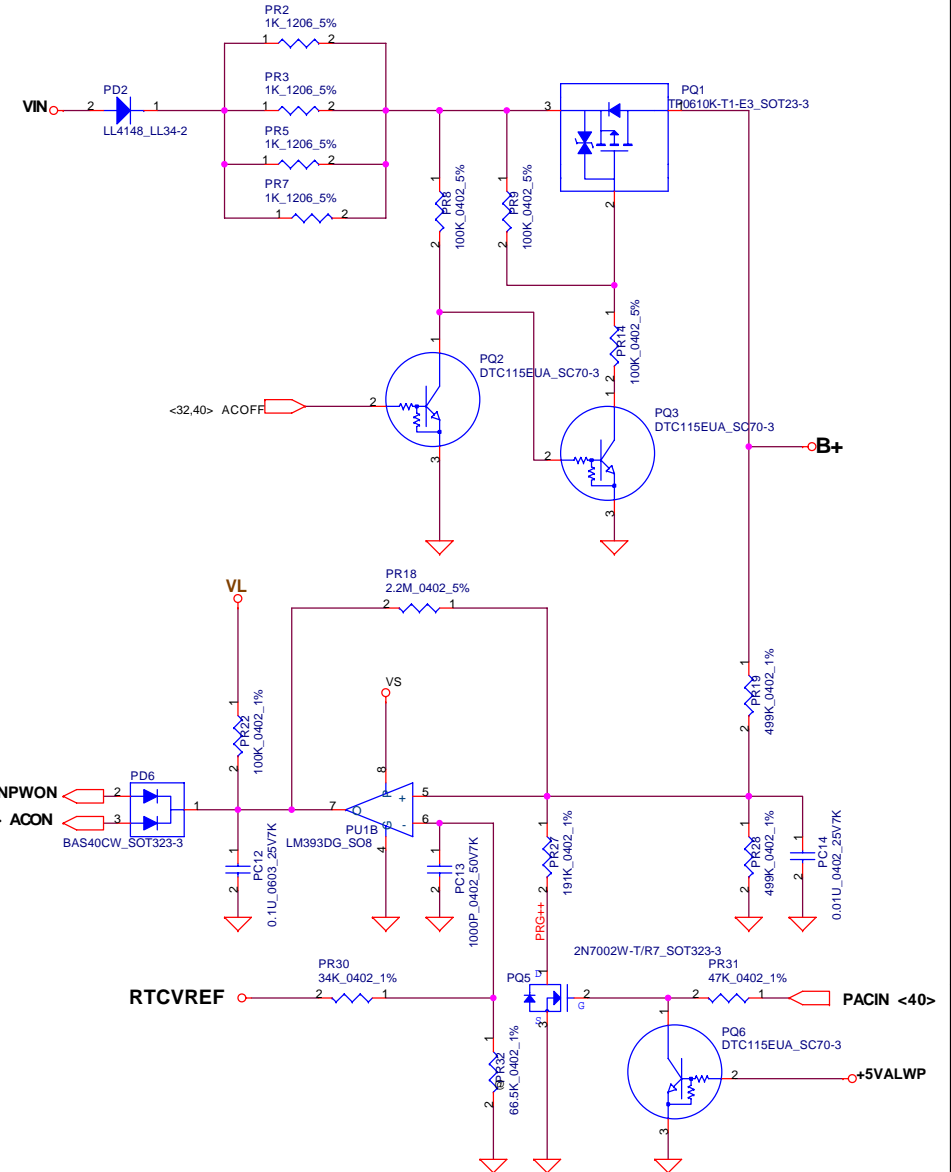


## ACIN

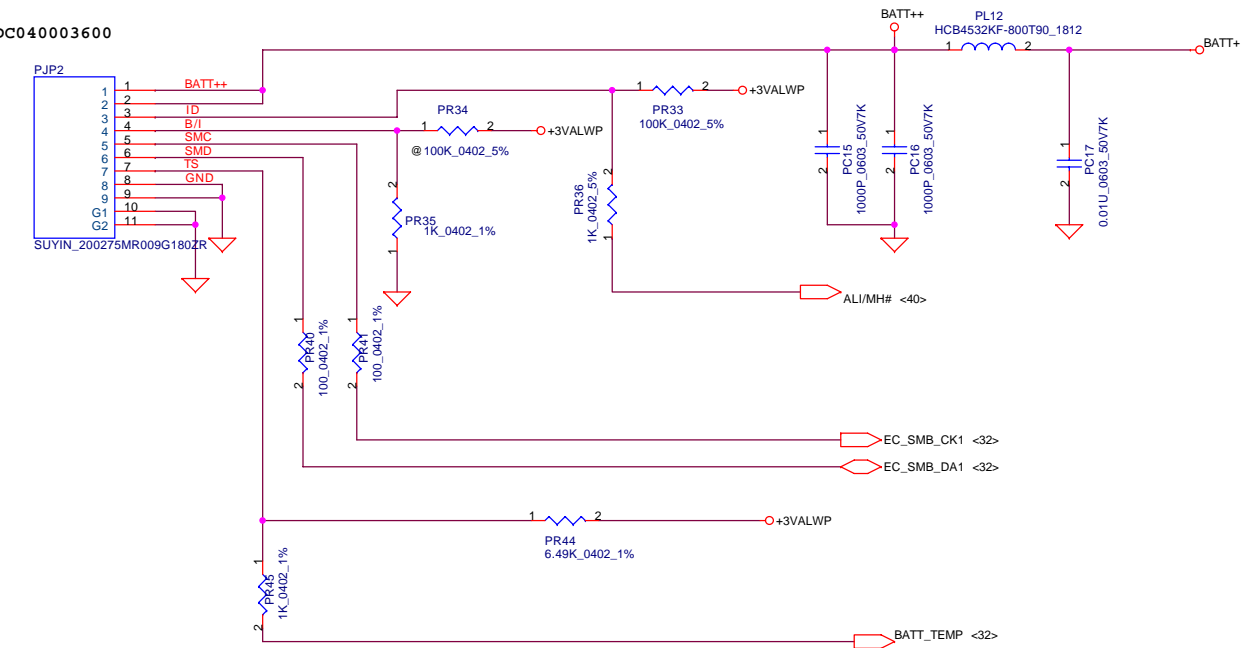
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

## BATT ONLY

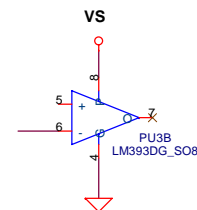
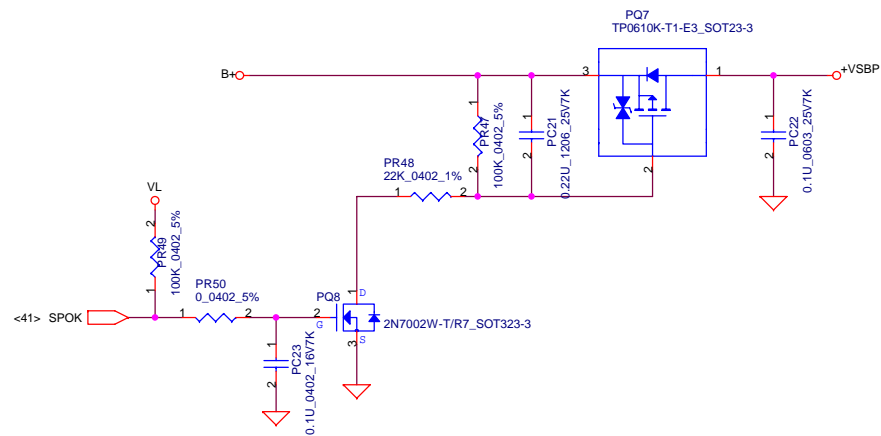
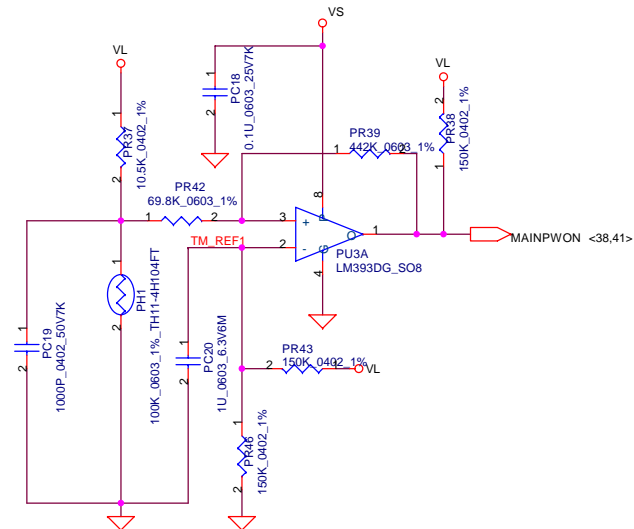
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



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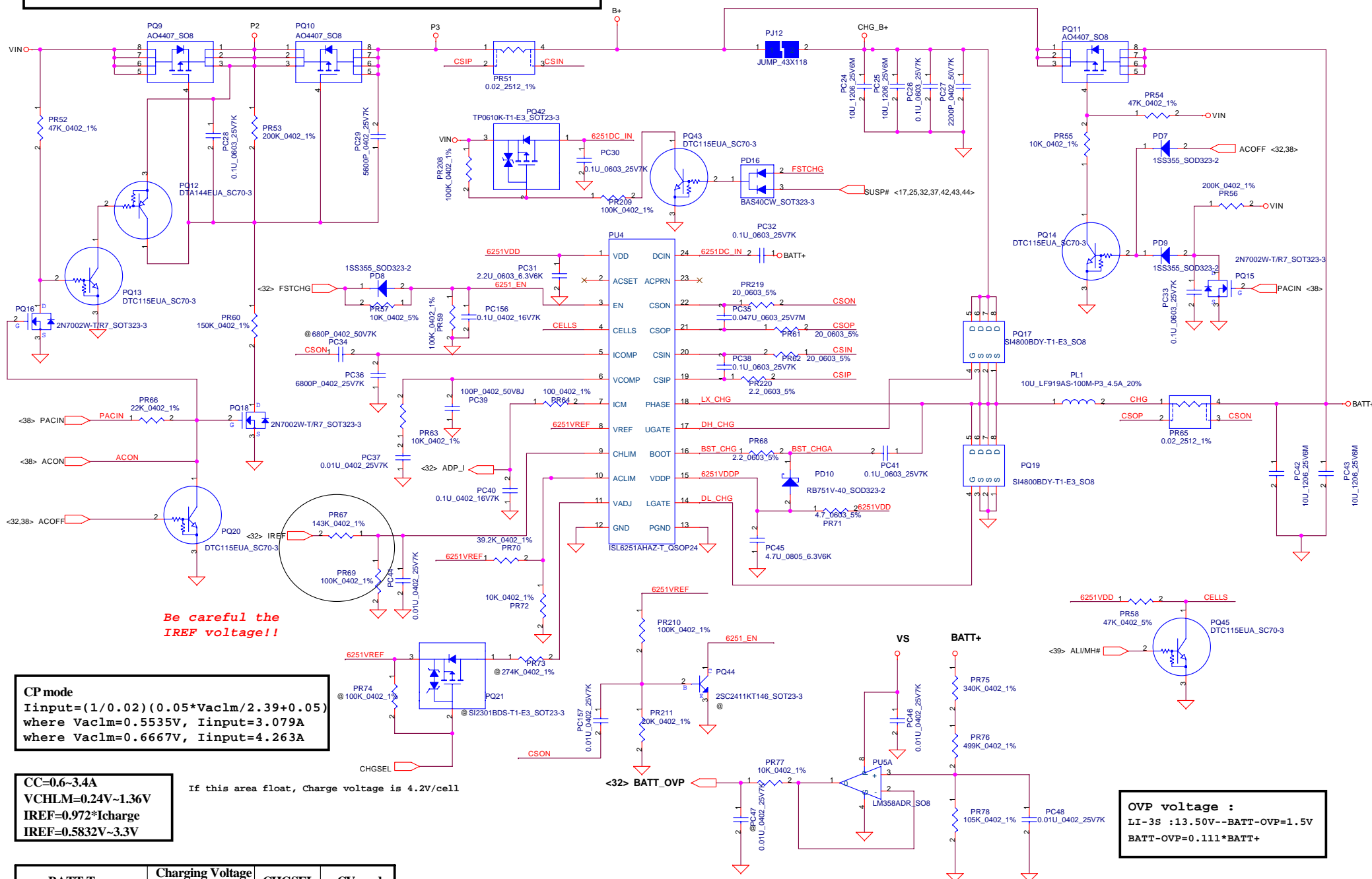
PH1 under CPU bottom side :  
CPU thermal protection at 87 degree C  
Recovery at 70 degree C



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65W, Iadapter=0~3.42A, Current sense=0.02ohm, PR70=39.2K, CP=3.079A  
90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR70=28.7K, CP=4.263A

$$ADP\_I = 19.9 * I_{\text{adapter}} * R_{\text{sense}}$$



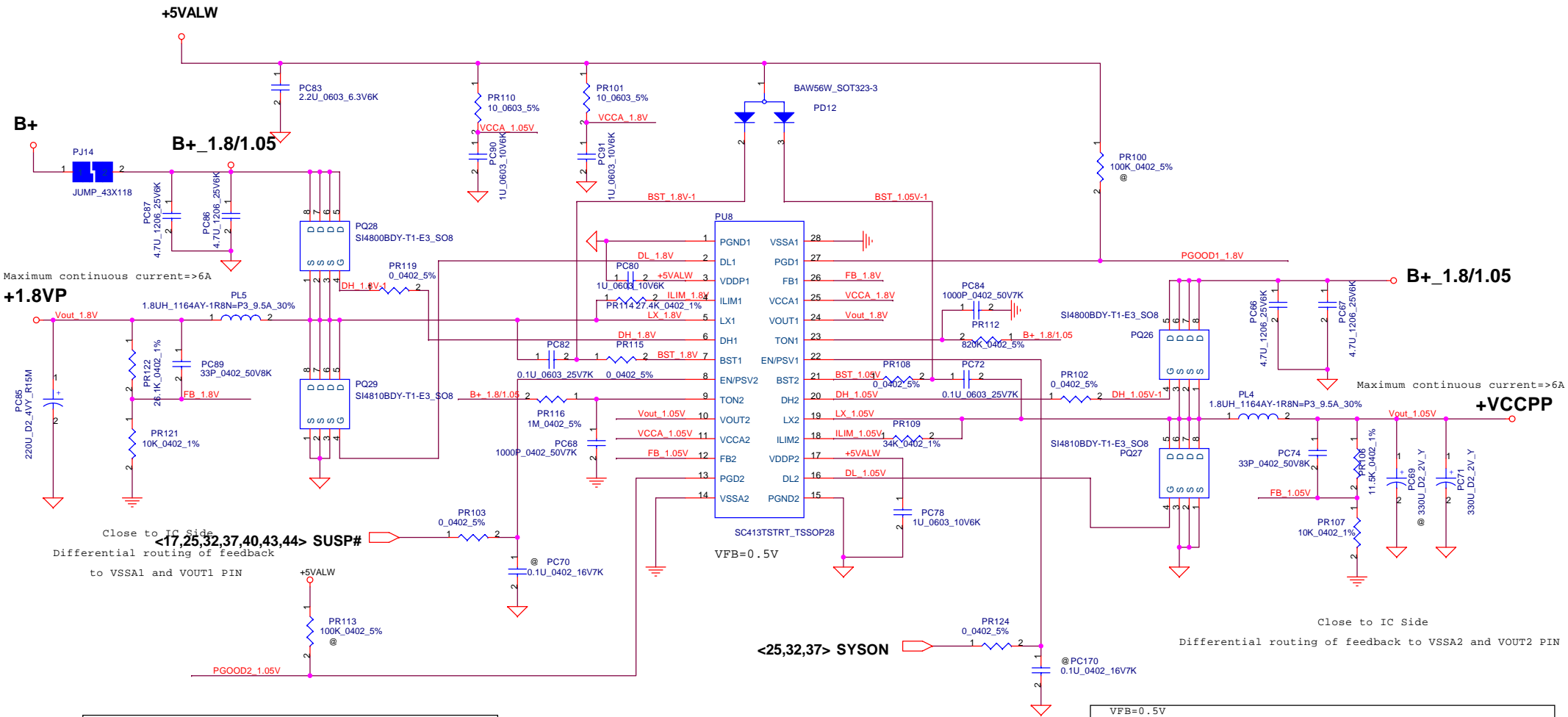
BATT Type	Charging Voltage (0x15)	CHGSEL	CV mode
2800mAH 3S pack	13050mV	LOW	12.90V
Normal 3S LI-ON Cells	12600mV	HIGH	12.60V

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Deciphered Date				2007/05/18				CHARGER			
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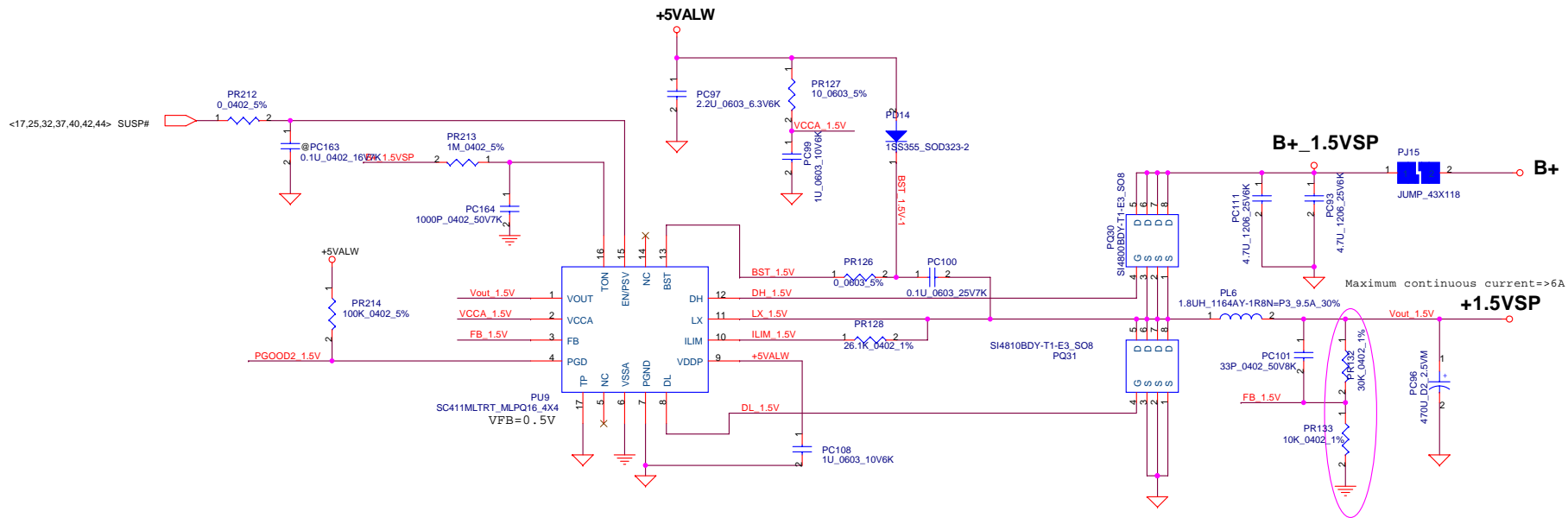
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Close to IC Side

Differential routing of feedback to VSSA2 and VOUT2 PIN

**VFB=0.5V, Ipeak=14.02A, Imax=9.814A**

The current rating of +1.05VSP include +VCC\_GFX current.

$V_o = V_{FB} * (1 + PR146 / PR147) = 1.05V$

$Ton = (3.3E-12 * (PR142 + 37K) * (Vout / VBat)) + 50ns = 0.239\mu s$

SI4810BDY:Rds(on) => Typ: 9mOhm

Max: 11.5 mOhm

$I_{valleymin} = 9 * 10E-6 * (PR145 / Rds(ON)_{max} * 1.5)$

**= 9 \* 10E-6 \* (26.1K / (0.0115 \* 1.5)) = 13.617A**

$I_{valleymax} = 11 * 10E-6 * (PR145 / Rds(ON)_{min} * 1.2)$

$= 11 * 10E-6 * (26.1K / (0.009 * 1.3)) = 20.076A$

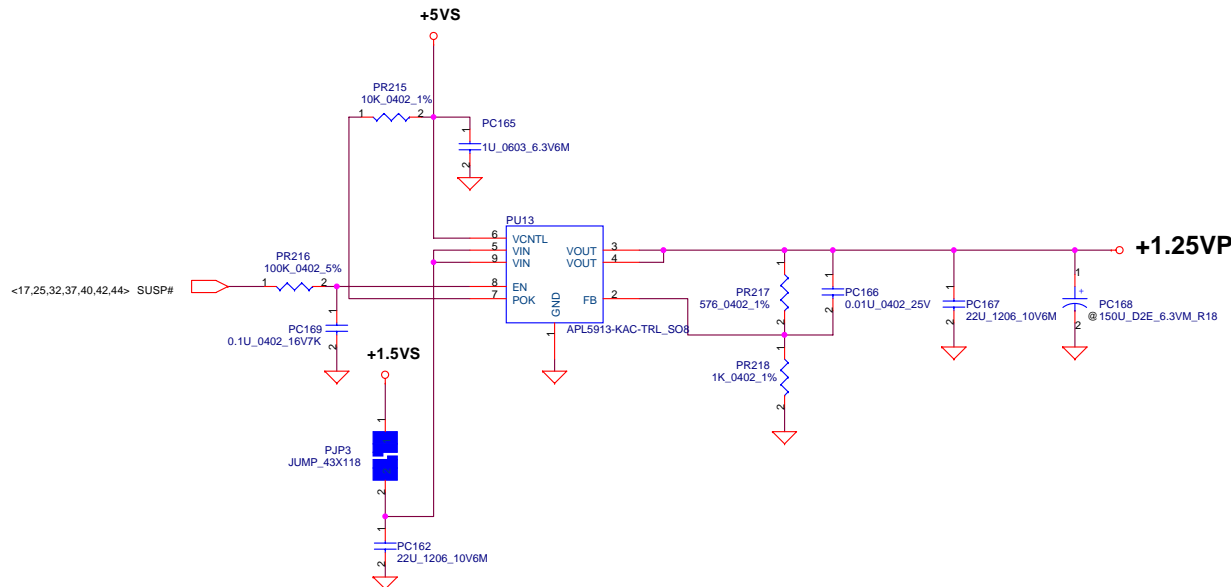
$I_{ripple} = (vin - vout) * (Ton / L) = 4.292A, 1/2 I_{ripple} = 2.146A$

$I_{ocp} = I_{valley} + I_{ripple} / 2$

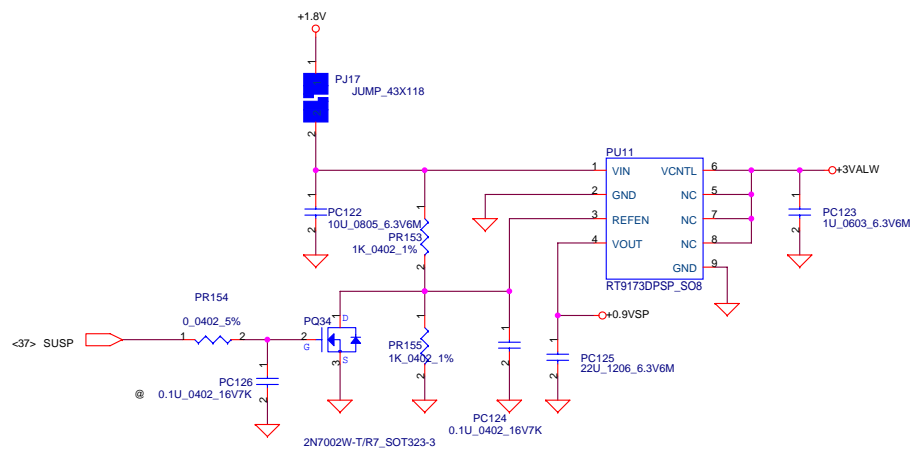
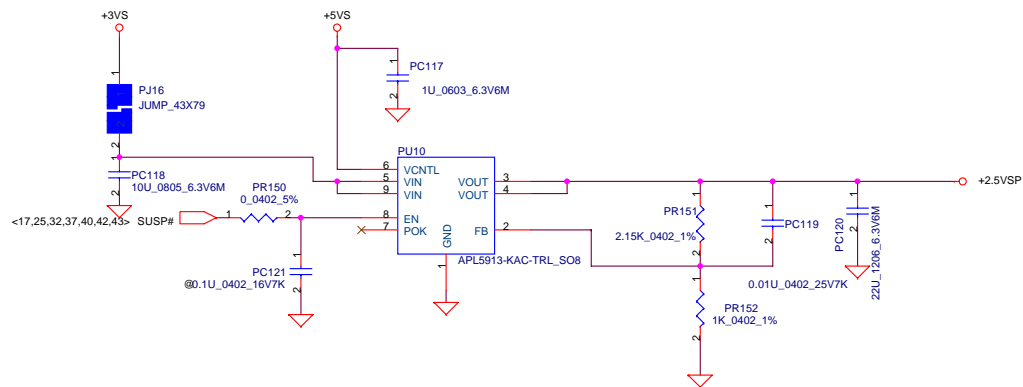
**OCP => 15.763A ~ 22.222A**

**Ipeak=2.91A, Imax=2A.**

$V_o = 0.8 * (1 + PR190 / PR191) = 1.2608V$



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POWER PIR

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